Exhibit U

Tab 2

File History of U.S. Patent No. 6,452,863 ("the '863 parent patent") not including the original disclosure

In the Application of:)
)
FARMWALD ET AL.) Group
) Art Unit:
Serial No: Continuation of 09/252,997)
) Before
Filed: JANUARY 27, 2000) Examiner:
)
Title: INTEGRATED CIRCUIT I/O USING A)
HIGH PERFORMANCE BUS INTERFACE)

Assistant Commissioner for Patents
Washington, DC 20231

POWER OF ATTORNEY BY ASSIGNEE, REVOCATION OF ALL PRIOR POWERS OF ATTORNEY AND CERTIFICATE UNDER 37 CFR 3.73(b)

Sir:

The undersigned, being empowered to sign this Power of Attorney, Revocation of All Previous Powers of Attorney and Certificate under 37 CFR 3.73(b) on behalf of Rambus, Inc., the assignee of the entire right, title and interest in the above-referenced application, hereby revokes all prior powers of attorney and hereby appoints Neil A. Steinberg, Reg. No. 34,735, with full power of substitution and revocation to prosecute this application and to transact all business before the United States Patent and Trademark Office in the above-referenced application.

Rambus, Inc., formerly a California corporation with a place of business at 4920A El Camino Real, Los Altos, California 94022, certifies that it is the assignee of the entire right, title and interest in the above-referenced patent application by virtue of an assignment from the inventors, Michael Farmwald and Mark Horowitz. The assignment of the parent patent application (Application Serial

Page -1-

No. 07/510,898) and all continuing and divisional application thereof to Rambus Inc. was filed on April 18, 1990 and recorded in the U.S. Patent and Trademark Office at Reel 5385, Frame 875.

The undersigned has reviewed all the documents in the chain of title of the above-referenced application and, to the best of the undersigned's knowledge and belief, title is in Rambus, Inc., the assignee identified above.
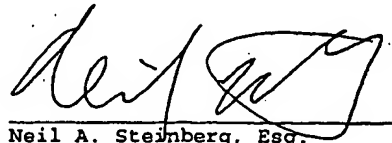
Please direct all correspondence in the above-referenced patent application to:

> Neil A. Steinberg, Esq.
> Rambus Inc.
> 2465 Latham Street
> Mountain View, California 94040
> Telephone: 650-944-7772
> Facsimile: 650-944-8080

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so make are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon.

Date: 1/27/00

Neil A. Steinberg, Esq.
Vice President
 Intellectual Property
Rambus Inc.

Page -2-

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
(Case No. P043D2C3C)

In the Application of:)	
)	
FARMWALD ET AL.)	Group
)	Art Unit:
Serial No: Continuation of 09/252,997)	
)	Before
Filed: JANUARY 27, 1999)	Examiner:
)	
Title: INTEGRATED CIRCUIT I/O USING A)	
HIGH PERFORMANCE BUS INTERFACE)	

Assistant Commissioner for Patents
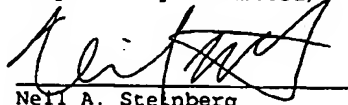Washington, DC 20231

REQUEST TO APPROVE DRAWING CHANGES

Dear Sir:

   Applicants seek to amend Figure 10 to more fully reflect the discussion in the specification, specifically, page 55, line 12-16 and page 58, lines 13-23. Attached is a photocopy of Figure 10 with the proposed changes indicated in red. No new matter has been added.

   Applicants respectfully request approval of the proposed changes. A new Figure 10 which incorporates the changes is also attached to hereto.

Respectfully submitted,

Date: January 27, 2000

Neil A. Steinberg
Reg. No. 34,735
650-944-7772

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
(Case No. P043D2C2C)

In the Application of:	)	
	)	
FARMWALD ET AL.	)	Group
	)	Art Unit:
Serial No: Continuation of 09/252,997	)	
	)	Before
Filed: JANUARY 27, 2000	)	Examiner:
	)	
Title: INTEGRATED CIRCUIT I/O USING A	)	
HIGH PERFORMANCE BUS INTERFACE	)	

Assistant Commissioner for Patents
Washington, DC   20231

<center>CROSS REFERENCE UNDER 37 C.F.R. §1.78 TO
POTENTIALLY RELATED APPLICATIONS</center>

Dear Sir:

The above-identified application may be related to the following application:

Application No. 09/252,998, filed on February 19, 1999 (still pending); Application No. 08/979,127, filed November 26, 1997, (now U.S. Patent 5,915,105); which is a continuation of Application No. 08/762,139, filed December 9, 1996 (now U.S. Patent 5,809,263); which is a continuation of Application No. 08/607,780, filed February 27, 1996 (now abandoned); which is a continuation of Application No. 08/222,646, filed March 31, 1994 (now U.S. Patent 5,513,327); which is a continuation of Application No. 07/954,945, filed September 30, 1992 (now U.S. Patent 5,319,755); which is a continuation of Application Serial No. 07/510,898 filed April 18, 1990 (now abandoned).
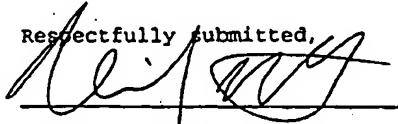
Application No. 09/252,993, filed on February 19, 1999 (still pending); which is a continuation of Application No. 08/798,525, filed on February 10, 1997 (still pending); which is a divisional of Application Serial No. 08/710,574, filed on

September 19, 1996 (now abandoned); which is a continuation of Application Serial No. 08/469,490 filed on June 6, 1995 (now abandoned); which is a continuation of Application Serial No. 07/847,961 filed on March 5, 1992 (now abandoned); which is a divisional of Application Serial No. 07/510,898 filed on April 18, 1990 (now abandoned).

All of these applications are assigned to the same assignee as the present application.

Date: January 27, 2000

Respectfully submitted,

Neil A. Steinberg
Reg. No. 34,735
703-787-9636

01-31-cc

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
REQUEST FOR FILING NEW UTILITY PATENT APPLICATION UNDER 37 CFR 1.53(b)
(Case No. P043D2C3C)

To the Assistant Commission for Patents
Washington, D.C.   20231

Sir:

Transmitted herewith for filing under 35 U.S.C. 111(a) and 37 C.F.R.
§1.53(b) is a new utility patent application for:

Title: INTEGRATED CIRCUIT I/O USING A
HIGH PERFORMANCE BUS INTERFACE

Inventors: Michael Farmwald
Mark Horowitz

This application is a CONTINUATION APPLICATION of:

Inventors: Michael Farmwald
Mark Horowitz

Ser. No.: 09/252,997   Art Unit: 2818

Filed: February 19, 1999   Examiner: T. Nguyen

Title: METHOD OF OPERATING A MEMORY
HAVING A VARIABLE DATA OUTPUT
LENGTH AND A PROGRAMMABLE REGISTER

To effect the above-requested filing today:

1.   Attached is a copy of the prior application as originally
     filed, including:
       [X] Specification, Claims, and Abstract (125 pages)
       [X] Drawings: 1 set of formal drawings having 14 sheets
       [X] Original Declaration and Power of Attorney (2 pages)

2.   Incorporation by Reference: The entire disclosure of the prior
     application, from which a copy of the oath or declaration is
     supplied, is considered as being part of the disclosure of the

Page 1

863 FH PG 0154

also revokes all other powers of attorney. Accordingly, kindly address all future communications to:

> Neil A. Steinberg, Esq.
> Rambus Inc.
> 2465 Latham Street.
> Mountain View, California 94040
>
> Telephone No. 650-944-7772
> Facsimile No. 650-428-0914

4. The Examiner's attention is directed to both the second paragraph of guideline (2) in MPEP 609 and to the last paragraph of MPEP 2001.06(b) and to the submission in the prior application of the Information Disclosure Statements and document copies filed in Application Serial Nos. 09/196,199 and 09/252,997.

5. Attached is a **PRELIMINARY AMENDMENT** which, among other things, cancels claims 1-150, and adds new claims 151-175. This Preliminary Amendment is to be entered <u>BEFORE</u> fee calculation.

6. **FILING FEE**
(BASED ON THE NUMBER OF CLAIMS AS FILED AND <u>CHANGED</u> BY PRELIMINARY AMENDMENT)

Basic Fee . . . . $ <u>690.00</u>

Additional Fees:

Surcharge for more than 20 total claims (<u>5</u> * $18) . . . . . $ <u>90.00</u>

Surcharge for more than 3 independent claims (<u>0</u> * 78) . . $ <u> - 0 -</u>

Surcharge for multiple dependent claims . . . . $ <u> - 0 -</u>

Total Filing Fee . . . . $ <u>780.00</u>

7. Manner of Payment:
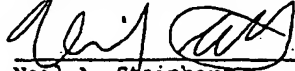
[ ] A check payable to the Commissioner of Patents and Trademarks, in the amount of $_____ is enclosed as payment of the Total Filing Fee.

[XX] Please charge my Deposit Account No. <u>50-0998</u> in the amount of <u>$780.00</u> to cover the above fees. A duplicate copy of this sheet is enclosed.

Page 2

[XX] The Commissioner is hereby authorized to charge any
fees which may be required, or credit any overpayment
to Deposit Account No. 50-0998. A duplicate copy of
this sheet is enclosed.

Respectfully submitted,

Date: January 27, 2000

Neil A. Steinberg
Reg. No. 34,735
650-944-7772

Page 3

EXPRESS MAIL CERTIFICATE OF MAILING

"Express Mail" mailing label number: ___EK100209508US_____

Date of Deposit:_____January 20, 2000___

I hereby certify that I am causing this paper or fee to be deposited with the United States Postal Service "Express Mail Post Office to Addressee" service on the date indicated above and that this paper or fee has been addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

Michiko Sites
_____

(Typed or printed name of person mailing paper or fee)

_Michiko Sites_____

(Signature of person mailing paper or fee)

___January 27, 2000_____

(Date signed)

EXPRESS MAIL CERTIFICATE OF MAILING

"Express Mail" mailing label number:___EK100209508US_____

Date of Deposit:_____January 20, 2000_____

I hereby certify that I am causing this paper or fee to be deposited with the United States Postal Service "Express Mail Post Office to Addressee" service on the date indicated above and that this paper or fee has been addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

Michiko Sites
_____
(Typed or printed name of person mailing paper or fee)

Michiko Sites
_____
(Signature of person mailing paper or fee)

January 27, 2000
_____
(Date signed)

Serial/Patent No.: Not Assigned Yet   Filing/Issue Date: Herewith
Title: Method of Operating a Memory Having a Variable Data Output Length and a Programmable Register
Atty. Docket No.: P043D2C3C   Date Mailed: January 27, 2000

The following has been received in the U.S. Patent & Trademark Office on the date stamped hereon:

☐ Amendment/Response (pgs.)	☐ Petition for Extension of Time (month(s))
☒ Preliminary Amendment (10 pgs.)	☐ Information Disclosure Statement & PTO 1449
☐ Application - Utility (pgs., with cover and abstract)	☐ Issue Fee Transmittal
☒ Application - Rule 1.53(b) Continuation (125 pgs.)	☐ Submission of Formal Drawings
☐ Application - Rule 1.53(b) Divisional (pgs.)	☐ Notice of Appeal
☐ Application - Rule 1.53(b) CIP (pgs.)	☐ Appeal Brief (pgs. in triplicate)
☐ Application - Rule 1.53(d) CPA (pgs.)	☐ Reply Brief
☐ Application - PCT (pgs.)	☐ Response to Notice of Missing Parts
☐ Application - Provisional (pgs.)	☒ Transmittal Letter (in duplicate)
☒ Drawings (14 sheets)	☐ Fee Transmittal (in duplicate)
☒ Declaration & POA (2 pgs.)	☒ Itemized Postcard
☐ Assignment & Cover Sheet	☐ Certificate of Mailing
☒ Power of Attorney	☐ Express Mail No. EK100209508US
☒ Other Cross Reference Under 37 C.F.R. 1.78	

Request to Approve drawing changes (2 pages)

In the Application of:)

     FARMWALD ET AL.   ) Group
) Art Unit:

Serial No: Continuation of 09/252,997   )
) Before

Filed: JANUARY 27, 2000   ) Examiner:
)

Title: INTEGRATED CIRCUIT I/O USING A   )
      HIGH PERFORMANCE BUS INTERFACE   )

Assistant Commissioner for Patents
Washington, DC   20231

PRELIMINARY AMENDMENT

Dear Sir:

    Prior to the examination of the above-referenced application, kindly amend the application as follows:

IN THE ABSTRACT:

    Please delete the Abstract of the Disclosure and substitute the attached Abstract of the Disclosure.

IN THE TITLE:

    Please delete the title and substitute --METHOD OF OPERATING A MEMORY DEVICE HAVING A VARIABLE DATA INPUT LENGTH--.

IN THE SPECIFICATION:

    On page 1, line 8, insert --This application is a continuation of Application No. 09/252,997 (still pending), now U.S. Patent No. 6,034,918 which is a

continuation of Application No. 09/196,199, filed on November 20,

now U.S. Patent No. 6,038,195

1998 ~~(still pending)~~, which is a continuation of Application No.

would 08/798,520, filed on February 10, 1997 (now U.S. Patent 5,841,580);

A3 which is a division of Application No. 08/448,657, filed May 24,

1995 (now U.S. Patent 5,638,334); which is a division of

Application No. 08/222,646, filed on March 31, 1994 (now U.S.

Patent 5,513,327); which is a continuation of Application No.

07/954,945, filed on September 30, 1992 (now U.S. Patent

5,319,755); which is a continuation of Application No. 07/510,898,

filed on April 18, 1990 (now abandoned).

On page 3, line 9, delete "micro-processor" and substitute
--microprocessor--.

On page 6, line 1, delete "4,646,279" and substitute
--4,646,270--.

On page 10, line 18, delete "Figure 7 shows" and substitute
--Figures 7a and 7b show--.

On page 10, line 21, delete "Figure 8 shows" and substitute --
Figures 8a and 8b show--.

On page 34, line 4, after "devices" insert --do--.

On page 41, line 1, delete "or" "and substitute -- or--.

On page 45, line 17, delete "Fig. 7" and substitute --Figures
7a and 7b--.

On page 47, line 2, delete "Figure 8" and substitute
--Figure 8a--.

On page 47, line 5, delete "from left to right" and substitute
-- from right to left--.

On page 47, line 8, delete "right" and substitute --left--.

Page 2

On page 47, line 9, delete the first "left" and substitute --right--.

On page 49, line 22, delete "primay" and substitute --primary--.

On page 54, line 13, delete "70" and substitute --69--.

On page 56, line 2, delete "Figurell" and substitute --Figure 11--.

On page 60, line 10, after "147" insert --A, B--.

IN THE CLAIMS:

Kindly cancel claims 1-150, without prejudice.

Kindly add the following claims:

-- 151. A method of controlling a memory device, wherein the memory device includes a plurality of memory cells, the method of controlling the memory device comprises:

providing first block size information to the memory device, wherein the first block size information defines a first amount of data to be input by the memory device in response to a write request; and

issuing a first write request to the memory device, wherein in response to the first write request the memory device inputs the first amount of data corresponding to the first block size information.

Page 3

152. The method of claim 151 wherein the memory device inputs the first amount of data synchronously with respect to an external clock signal.

153. The method of claim 151 further including:

providing second block size information to the memory device, wherein the second block size information defines a second amount of data to be input by the memory device in response to a write request; and

issuing the second write request to the memory device, wherein in response to the second write request, the memory device inputs the amount of data corresponding to the second block size information.

154. The method of claim 151 wherein the first block size information and the first write request are included in a request packet.

155. The method of claim 154 wherein the first block size information and the first write request are included in the same request packet.

156. The method of claim 151 further including providing the amount of data corresponding to the first block size information to the memory device.

Page 4

157. The method of claim 156 wherein the data is provided to the memory device after a delay time transpires.

158. The method of claim 156, wherein the delay time is representative of a number of clock cycles of a clock signal.

159. The method of claim 151 wherein the first block size information is a binary representation of the first amount of data to be input in response to the first write request.

160. The method of claim 151 wherein the first amount of data corresponding to the first block size information is input synchronously during a plurality of clock cycles of the external clock signal.

161. A method of operation of a memory device, wherein the memory device includes a plurality of memory cells, the method of operation of the memory device comprises:

receiving first block size information from a bus controller, wherein the first block size information defines a first amount of data to be input by the memory device in response to a write request;

receiving a first write request from the bus controller; and

inputting the first amount of data corresponding to the first block size information in response to the first write request.

Page 5

162. The method of claim 161 wherein the data corresponding to the first block size information is sampled synchronously with respect to the external clock signal.

163. The method of claim 161 further including:
  receiving second block size information, wherein the second block size information defines a second amount of data to be input in response to a second write request;
  receiving a second write request from the bus controller; and
  inputting the amount of data corresponding to the second block size information, in response to the second write request.

164. The method of claim 161 wherein the first block size information and the first write request are included in a request packet.

165. The method of claim 164 wherein the first block size information and the first write request are included in the same request packet.

166. The method of claim 161 wherein the first block size information is a binary representation of the first amount of data to be input in response to the first write request.

167. The method of claim 161 wherein the first amount of data corresponding to the first block size information is input

3   synchronously during a plurality of clock cycles of an external

4   clock signal.

168. The method of claim 161 further including generating an
internal clock signal using a delay locked loop and an external
clock signal wherein the first amount of data corresponding to the
first block size information is input synchronously with respect to
the internal clock signal.

169. The method of claim 161 further including generating
first and second internal clock signals using clock generation
circuitry and an external clock signal wherein the first amount of
data corresponding to the first block size information is input
synchronously with respect to the first and second internal clock
signals.

170. The method of claim 169 wherein the first and second
internal clock signals are generated by a delay lock loop.

171. A method of operation of an integrated circuit, wherein
the integrated circuit includes a memory array having a plurality
of memory cells, the method of operation comprises:

receiving block size information, wherein the block size
information defines a first amount of data to be input ~~from a bus~~
in response to a write request;

receiving a first write request; and

Page 7

8   inputting the first amount of data corresponding to the block
9   size information in response to the first write request.

277. The method of claim 171 further including storing the
first amount of data corresponding to the block size information in
the memory array.

1   173. The method of claim 171 wherein the block size
2   information and the first write request are included in a request
3   packet.

174. The method of claim 171 wherein the first block size
information is a binary representation of the first amount of data
to be input in response to the first write request.

175. The method of claim 171 wherein the first block size
information is provided by a controller.--

REMARKS

This Preliminary Amendment seeks to place this application in
condition for allowance. This application is a continuation of
Application No. 09/252,997, which is a continuation of Application
No. 09/196,199. Application Serial Nos. 09/252,997 and 09/196,199
are pending.

Page 8

Applicants request priority to Application Serial No. 07/510,898, filed April 18, 1990, now abandoned. Applicants request such priority through Application No. 09/252,997 (still pending), which is a continuation of Application No. 09/196,199, filed on November 20, 1998 (still pending), which is a continuation of Application No. 08/798,520, filed on February 10, 1997 (now U.S. Patent 5,841,580); which is a division of Application No. 08/448,657, filed May 24, 1995 (now U.S. Patent 5,638,334); which is a division of Application No. 08/222,646, filed on March 31, 1994 (now U.S. Patent 5,513,327); which is a continuation of Application No. 07/954,945, filed on September 30, 1992 (now U.S. Patent 5,319,755); which is a continuation of Application No. 07/510,898, filed on April 18, 1990 (now abandoned).

Accordingly, Applicants claim the benefit of the filing date of Application Serial No. 07/510,898 -- i.e., April 18, 1990. The specification has been amended to identify the continuation or related U.S. application data identified above. No new matter has been added.

In this continuation application, Applicants present new claims which set forth novel and unobvious features of Applicants' invention. Applicants submit new claims 151-175 to more fully protect the instant invention. No new matter has been added.

The newly submitted claims are believed to be fully supported by the specification -- see, for example, Figures 2 and 10-13; page 14, line 3 to page 15, line 2; page 15, lines 18 to page 16, line 7; page 20, line 20 to page 21, line 20; page 23, line 6 to page 24, line 2; page 27, line 23 to page 28, line 20; page 46, line 19

Page 9

to page 48, line 17; page 53, line 23 to page 59, line 2; page 71, line 23 to page 72, line 21, page 73, lines 20 to page 74, line 31; and page 115, lines 10-22.

Applicants have also amended the specification to correct obvious spelling, typographical and grammatical errors. No new matter has been added.
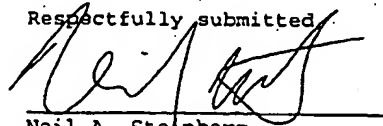
In addition, a new Abstract of the Disclosure is attached hereto. No new matter has been added.

Finally, accompanying this Preliminary Amendment is a Request to Approve Drawing Changes. In that Request, Applicants seek to amend Figure 10 to more fully reflect the discussion in the specification, in particular, page 55, lines 12-16 and page 58, lines 13-23. The proposed changes are indicated in red. No new matter has been added. Applicants respectfully request that the Examiner approve the proposed changes to Figure 10. A new Figure 10 which incorporates the changes is also attached to the Request.

CONCLUSION

Applicants request entry of the foregoing amendment prior to examination of this application. Applicants submit that all of the claims present patentable subject matter. Accordingly, Applicants respectfully request allowance of all of the claims.

Respectfully submitted

Date: January 27, 2000

Neil A. Steinberg
Reg. No. 34,735
301-229-7706

Page 10

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
(Case No. P043D2C3C)

In the Application of:)
)
        FARMWALD et al.   )
)
Serial No: 09/492,982   )   Group
)   Art Unit:
Filed: JANUARY 27, 2000   )
)   Before
Title: INTEGRATED CIRCUIT I/O USING A)   Examiner:
         HIGH PERFORMANCE BUS INTERFACE)
)

Assistant Commissioner for Patents
Washington, DC 20231

                    INFORMATION DISCLOSURE STATEMENT

Dear Sir:

        In compliance with the duty of disclosure set forth in 37 C.F.R.

§1.56, submitted herewith is a modified Form PTO-1449, including a copy

of all of the documents cited therein -- except for those references

which were provided or cited during the prosecution of App. S/N

09/252,997 to which priority is claimed (See 37 C.F.R. §1.98(d)).

        It is believed that the Examiner may find the documents cited in

the modified Form PTO-1449 material to the patentability of one or more

of the claims in the above-captioned application. Accordingly, it is

respectfully requested that the Examiner make his consideration of

these references formally of record with the initial Office Action.

                                    Respectfully submitted,

Date: February 28, 2000

                                    Neil A. Steinberg, Esq.
                                    Reg. No. 34,735
                                    (650) 944-7772

PTO-1449 (Modified) 13	ATTY. DOCKET NO. P043D2CJC	SERIAL NUMBER 09/492,982
U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	APPLICANT(S) FARMWALD ET AL.	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	FILING DATE JANUARY 27, 2000	GROUP ART UNIT

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
TNT	4,945,516	07/31/90	Kashiyama	365	189.05	
	4,807,189	02/21/89	Pinkham et al.	365	220	
	4,586,167	04/21/86	Fujishima et al.	365	189.05	
	4,337,523	06/29/82	Hotta et al.	365	194	
	4,825,416	05/25/89	Tam et al.	365	194	
	4,750,839	06/14/88	Wang et al.	365	233	
	4,513,370	04/23/85	Ziv et al.	709	253	
	4,099,231	07/04/78	Kotok et al.	711	168	
TNT	5,175,835	12/29/92	Beighe et al.	711	212	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER TAN T. NGUYEN	DATE CONSIDERED 05/16/00

EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant.

PTO-1449 (Modified)	ATTY. DOCKET NO. P043D2C3C	SERIAL NUMBER 09/492,982
U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	APPLICANT(S) FARMWALD ET AL.	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	FILING DATE JANUARY 27, 2000	GROUP ART UNIT

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
TNT	4,891,791	01/02/90	Iijima	365	189.01	
	4,092,665	05/30/78	Saran	341	63	
	5,093,807	03/03/92	Hashimoto et al.	365	230.09	
	3,882,470	05/06/71	Hunter	365	200	
	5,083,296	01/21/92	Hara et al.	365	230.02	
	4,792,926	12/20/88	Roberts	365	189.02	
	4,719,602	01/12/88	Hag et al.	365	189.02	
	4,785,394	11/15/88	Fischer	710	114	
	5,083,260	01/21/92	Tsuchiya	710	113	
	4,954,987	09/04/90	Auvinen et al.	365	189.02	
	4,675,850	06/23/87	Kumanoya et al.	365	189.08	
TNT	4,788,667	11/29/88	Nakano et al.	365	193	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

TNT	M. Bazes et al., "A Programmable NMOS DRAM Controller for Microcomputer Systems with Dual-Port Memory and Error Checking and Correction", IEEE Journal of Solid State Circuits, vol. 18 No. 2, pp. 164-172 (Apr. 1983)
TNT	A. Agarwal, "An Evaluation of Directory Schemes for Cache Coherence", IEEE document pp.280-289 (1988)
TNT	D. Kawley, "SUPERFAST BUS SUPPORTS SUPERFAST TRANSACTIONS", High Performance Systems, pp 90-94 (Sept. 89)
TNT	H. L. Kalter et al., "A 50-ns 16Mb DRAM with a 10-ns Data Rate and On-Chip ECC", IEEE Journal of Solid State Circuits, vol. 25 No. 5, pp. 1118-1128 (Oct 1990)
TNT	S. Watanabe et al., "AN Experimental 16-Mbit CMOS DRAM Chip with a 100-MHz Serial READ/WRITE Mode", IEEE Journal of Solid State Circuits, vol. 24 No. 3, pp. 763-770 (June 1982)

EXAMINER Tan T. Ninten	DATE CONSIDERED 05/16/00

EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant.

PTO-1449 (Modified) 3.	ATTY. DOCKET NO. P043D2CJC	SERIAL NUMBER 09/492,982
U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	APPLICANT(S) FARMWALD ET AL.	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	FILING DATE JANUARY 27, 2000	GROUP ART UNIT

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
TNT	4,445,204	04/24/84	Nishiguchi	365	194	
	4,821,226	04/11/89	Christopher et al.	365	230.03	
	4,882,712	11/21/89	Ohno et al.	365	206	
	4,951,251	08/21/90	Yamaguchi et al.	365	189.02	
	4,928,265	12/29/92	Deighe et al.	365	189.01	
	5,107,465	04/21/92	Fung et al.	365	230.3	
	5,206,833	04/27/93	Lee	365	233	
TNT	4,953,128	08/28/90	Kawai et al.	365	194	

(Stamp: O I P E MAR 0 2 2000 PATENT & TRADEMARK)

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

TNT	T.L. Jeremiah et al., "SYNCHRONOUS PACKET SWITCHING MEMORY AND I/O CHANNEL," IBM Tech. Disc. Bul. Vol. 24, No. 10, pp. 4986-4987 (Mar. 1982)
TNT	L. R. Metzegzs, "A 16K CMOS PROM with Polysilicon Fusible Links", IEEE Journal of Solid State Circuits, vol. 18 No. 5, pp. 562-567 (Oct. 1983)
TNT	A. Yuen et. al., "A 32K ASIC Synchronous RAM Using a Two-Transistor Basic Cell", IEEE Journal of Solid State Circuits, vol. 24 No. 1, pp. 57-61 (Feb. 1989)
TNT	D.T. Wong et. al., "An 11-ns 8Kx18 CMOS Static RAM with 0.5-μm Devices", IEEE Journal of Solid State Circuits, vol. 23 No. 5, pp. 1095-1103 (Oct. 1988)
TNT	T. Williams et. al., "An Experimental 1-Mbit CMOS SRAM with Configurable Organization and Operation", IEEE Journal of Solid State Circuits, vol. 23 No. 5, pp. 1085-1094 (Oct. 1988)

EXAMINER TAN T. NGUYEN	DATE CONSIDERED 05/16/00

EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant.

PTO-1449 (Modified)	4	ATTY. DOCKET NO. P043D2C3C	SERIAL NUMBER 09/492,982
U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		APPLICANT(S) FARMWALD ET AL.	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT		FILING DATE JANUARY 27, 2000	GROUP ART UNIT

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
TNT	5,140,688	08/18/92	White et al.	345	550	
	5,018,111	05/21/9	Midland	365	233	
	4,734,880	03/29/8	Collins	711	105	
	4,183,095	01/08/80	Ward	365	189.02	
	4,975,872	12/04/90	Zaiki	365	49	
	5,016,226	05/14/91	Hiwada et al.	365	233	
TNT	5,109,498	04/28/92	Kamiya et al.	395	425	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

TNT	D. Jones, "Synchronous static ram", Electronics and Wireless World, vol.93, no.1622, pp. 1243-4 (Dec. 87)
TNT	F. Miller et al., "HIGH FREQUENCY SYSTEM OPERATION USING SYNCHRONOUS SRAMS", Midcon/87 Conference Record, pp. 430-432, Chicago, IL, USA, 15-17 Sept. 1987
TNT	K. Ohta, "A 1-Mbit DRAM with 33-MHz Serial I/O Ports", IEEE Journal of Solid State Circuits, vol. 21 No. 5, pp. 649-654 (Oct. 1986)
TNT	K. Nogami et. al., "A 9-ns HIT-Delay 32-kbyte Cache Macro for High-Speed RISC", IEEE Journal of Solid State Circuits, vol. 25 No. 1, pp. 100-108 (Feb. 1990)
TNT	F. Towler et. al., "A 128x 6.5ns Access/ 5ns Cycle CMOS ECL Static RAM", 1989 IEEE International Solid State Circuits Conference, (Feb. 1989)
TNT	M. Kimoto, "A 1.4ns/64kb RAM with 85ps/3680 Logic Gate Array", 1989 IEEE Custom Integrated Circuits Conference

EXAMINER Tan T. Nguyen	DATE CONSIDERED 05/16/00

EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant.

PTO-1449 (Modified)	ATTY. DOCKET NO. P043D2C3C	SERIAL NUMBER 09/492,982
U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	APPLICANT(S) FARMWALD ET AL.	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	FILING DATE JANUARY 27, 2000	GROUP ART UNIT

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
TNT	4,807,189	02/21/89	Pinkham et al.	365	189.05	
	4,092,663	05/30/78	Soren	341	63	
TNT	4,799,199	01/17/89	Scales, III et al.	365	230.06	
	5,142,637	09/25/92	Harlin et al.	345	425	
	5,148,523	09/15/92	Harlin et al.	345	519	
	4,954,987	09/04/90	Auvinen et al.	365	189.02	
	4,675,850	06/23/87	Nakano et al.	365	230.01	
	4,788,667	05/22/90	Higuchi	365	193	
	4,937,734	06/26/90	Bechtolsheim	711	202	
	4,680,738	07/14/87	Tam	365	239	
	4,845,664	07/04/89	Aichelmann, Jr. et al.	364	900	
TNT	4,920,483	04/24/90	Pogue et al.	364	200	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

TNT	D. Wendell et al. "A 3.5ns, 2Kx9 Self Timed SRAM", 1990 IEEE Symposium on VLSI Circuits (Feb 1990)
	M. Bazes et al., "A Programmable NMOS DRAM Controller for Microcomputer Systems with Dual-Port Memory and Error Checking and Correction", IEEE Journal of Solid State Circuits, vol. 18 No. 2, pp. 164-172 (Apr. 1983)
TNT	R. Schmidt, "A memory Control Chip fo Formatting Data into Blocks Suitable for Video Applications"; IEEE Transactions on Circuits and Systems, vol. 36, No. 10 (Oct. 1929)
TNT	D. K. Morgan "The CVAX CMCTL – A CMOS Memory Controller Chip", Digital Technical Journal, No. 7 (Aug. 1988)
TNT	T.C. Poon et. al.. "A CMOS DRAM-Controller Chip Implementation", IEEE Journal of Solid State Circuits, vol. 22 No. 3, pp. 491-494 (June 1987)
TNT	K. Numata et. al. " New Nibbled-Page Architecture for High Density DRAM's", IEEE Journal of Solid State Circuits, vol. 24 No. 4, pp. 903-904 (Aug. 1989)
TNT	E.H. Frank "The SBUS: Sun's High Performance System Bus for RISC Workstations" Sun Microsystems Inc. 1990

EXAMINER Tan T. Nguyen	DATE CONSIDERED 05/16/00

EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered.
Include copy of this form with next communication to applicant.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
(P0043D2C3C)

In re Application of:)
)
FARMWALD ET AL.   )
)   Art Unit:
Serial No: 09/492,982)
)
Filed: JANUARY 27, 2000)   Examiner:
)
Title: INTEGRATED CIRCUIT I/O USING A HIGH)
       PERFORMANCE INTERFACE)

Commissioner of Patents and Trademarks
Washington, D.C. 20231

Dear Sir:

   With respect to the above-identified application, transmitted herewith is an INFORMATION DISCLOSURE
STATEMENT.

Fees:	
Submission of Information Disclosure Statement under 37 CFR §1.97(b)	$0
TOTAL FEE DUE:	$0

[ ]   A check payable to the Commissioner of Patents and Trademarks, in the amount of $_____ is enclosed as
       payment of the Total Fee Due.

[ ]   Please charge my Deposit Account No. 50-0998 in the amount of $240.00 to cover the above fees. A duplicate copy
       of this sheet is enclosed.

[XX] The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any
       overpayment to Deposit Account No. 50-0998. A duplicate copy of this sheet is enclosed.

                                        Respectfully submitted,

Date: February 28, 2000

                                        By:
                                        Neil A. Steinberg
                                        Registration No. 34,735
                                        650-944-7772

28 ∞
~~0260~~

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
(Case No. P043D2C3C)

In the Application of:

FARMWALD, ET AL.

Serial No.: 09/492,982

Filed: JANUARY 27, 2000

Title: INTEGRATED CIRCUIT I/O USING A
HIGH PERFORMANCE INTERFACE

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RECEIVED

APR 0 3 2000

TECHNOLOGY CENTER 2800

Assistant Commissioner for Patents
Washington, DC 20231

Certificate of Mailing Under 37 CFR 1.8

I hereby certify that the attached 1) Transmittal of Information Disclosure

Statement (1 page and 1 copy thereof), and 2) Information Disclosure Statement

(6 pages and documents cited in IDS) is/are being deposited with the United States

Postal Service with sufficient postage as first class U.S. mail in an envelope addressed

to:

Assistant Commissioner for Patents
Washington, D.C. 20231

on February 28, 2000.

(Signature)

Michiko Sites

(Print Name of Person Signing Certificate)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR		ATTORNEY DOCKET NO.
09/492.982	01/27/00	FARMWALD	M	P043D2C3C

MMC1/0519

┌
Neil A Steinberg Esq
Rambus Inc
2465 Latham Street
Mountain View CA 94040
┐

EXAMINER
NGUYEN. T

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 05/19/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No. 09/472,982	Applicant(s) FARMWALD et al.
	Examiner TAN T. NGUYEN	Group Art Unit 2818

—The *MAILING DATE* of this communication appears on the cover sheet beneath the correspondence address—

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE __-3-__ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

☑ Responsive to communication(s) filed on __01/27/02__

☐ This action is FINAL.

☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

☑ Claim(s) __151-175__ is/are pending in the application.

　Of the above claim(s) __1-150__ is/are withdrawn from consideration.

☐ Claim(s)_____ is/are allowed.

☐ Claim(s)_____ is/are rejected.

☐ Claim(s)_____ is/are objected to.

☐ Claim(s)_____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☑ The proposed drawing correction, filed on __01/27/00__ is ☑ approved ☐ disapproved.

☐ The drawing(s) filed on_____ is/are objected to by the Examiner.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119 (a)-(d)

☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

　☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

　☐ received.

　☐ received in Application No. (Series Code/Serial Number)_____.

　☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

　*Certified copies not received:_____

Attachment(s)

☑ Information Disclosure Statement(s), PTO-1449, Paper No(s). __3__　　☐ Interview Summary, PTO-413

☑ Notice of Reference(s) Cited, PTO-892　　　　　　　　　　　　　　☐ Notice of Informal Patent Application, PTO-152

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948　　　　　☐ Other_____

Office Action Summary

U.S. Patent and Trademark Office
PTO-326 (Rev. 9-97)

Part of Paper No. __4__

*U.S. GPO: 1998-454-457/87505

1.   The Preliminary amendment filed by Applicants on January 27, 2000 has been received.

2.   The Information Disclosure Statement submitted on March 2, 2000 has been received and

fully considered.

3.   The nonstatutory double patenting rejection is based on a judicially created doctrine
grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or
improper timewise extension of the "right to exclude" granted by a patent and to prevent possible
harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed.
Cir. 1993), *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686
F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA
1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).
        A timely filed terminal disclaimer in compliance with 37 CFR 1.321© may be used to
overcome an actual or provisional rejection based on a nonstatutory double patenting ground
provided the conflicting application or patent is shown to be commonly owned with this
application. See 37 CFR 1.130(b).
        Effective January 1, 1994, a registered attorney or agent of record may sign a terminal
disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4.   Claims 152-156, 159-160, 161-167, 171-175 are rejected under the judicially created

doctrine of double patenting over claims 2-5, 13, 20-23, 29 of U. S. Patent No. 6,034,918 since

the claims, if allowed, would improperly extend the "right to exclude" already granted in the

patent.

        The subject matter claimed in the instant application is fully disclosed in the patent and is

covered by the patent since the patent and the application are claiming common subject matter, as

follows:

        Claims 2-5, 13, 20-23, 29 of U. S. Patent No 6,034,918 recite first block size information

and second block size information which define a first and second amount of data to be input by

the memory device in response to a first and second write request. the first block size information

and the first write request are included in a same request packet.

Furthermore. there is no apparent reason why applicant was prevented from presenting

claims corresponding to those of the instant application during prosecution of the application

which matured into a patent. See *In re Schneller*, 397 F.2d 350. 158 USPQ 210 (CCPA 1968).

See also MPEP § 804.

5.   Claims 157-158. 168-170 are rejected under the judicially created doctrine of obviousness-

type double patenting as being unpatentable over claims 16-17 and 33 of U.S. Patent No.

6,034,918. Although the conflicting claims are not identical. they are not patentably distinct from

each other because claims 157-158 and 168-170 of the present application claiming step of

generating internal clock signal using delay locked loop and an external clock signal for an input

operation. while claims 16-17 and 33 of U.S. Patent No. 6,034,918 claim step of generating an

internal clock signal for an output operation.

It would have been obvious to a person of ordinary skill in the art at the time the invention

was made to modify the method of controlling the memory device of U.S. Patent No. 6,034,918

by generating the internal clock signal for both input and output operations.

The rationale is as follow: A person of ordinary skill in the art would have been motivated

to use the same components to generate internal clock signal for both input and output operation

to simplify the circuitry of the memory device

6.   Any inquiry concerning this communication or earlier communications from the examiner

should be directed to Tan T. Nguyen whose telephone number is (703) 308-1298. The examiner

can normally be reached on Monday to Friday from 08:00 AM to 04:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor,

Mr. David C. Nelms, can be reached on (703) 308-4910. The fax phone number for the

organization where this application or proceeding is assigned is (703) 308-7724.

Any inquiry of a general nature or relating to the status of this application or proceeding

should be directed to the receptionist whose telephone number is (703) 308-0956.

Tan T. Nguyen
Primary Examiner
Art Unit 2818
May 17, 2000

T.N
05/17/2000

NOTICE OF DRAFTSPERSON'S
PATENT DRAWING REVIEW

The drawing(s) filed (insert date) 1/27/00 are:

A. ☐ Approved by the Draftsperson under 37 CFR 1.84 or 1.152.

B. ☒ objected to by the Draftsperson under 37 CFR 1.84 or 1.152 for the reasons indicated below. The Examiner will require submission of new, corrected drawings when necessary. Corrected drawing must be submitted according to the instructions on the back of this notice.

1. DRAWINGS. 37 CFR 1.84(a): Acceptable categories of drawings:
   Black ink. Color.
   ___ Color drawings are not acceptable until petition is granted.
   Fig(s) ___
   ___ Pencil and non black ink not permitted. Fig(s) ___
2. PHOTOGRAPHS. 37 CFR 1.84 (b)
   ___ 1 full-tone set is required. Fig(s) ___
   ___ Photographs not properly mounted (must use bryatol board or photographic double-weight paper). Fig(s) ___
   ___ Poor quality (half-tone). Fig(s) ___
3. TYPE OF PAPER. 37 CFR 1.84(e)
   ___ Paper not flexible, strong, white, and durable.
   Fig(s) ___
   ___ Erasures, alterations, overwritings, interlineations, folds, copy machine marks not accepted. Fig(s) ___
   ___ Mylar, velum paper is not acceptable (too thin).
   Fig(s) ___
4. SIZE OF PAPER. 37 CFR 1.84(f): Acceptable sizes:
   ___ 21.0 cm by 29.7 cm (DIN size A4)
   ___ 21.6 cm by 27.9 cm (8 1/2 x 11 inches)
   ___ All drawing sheets not the same size.
   Sheet(s) ___
   ___ Drawings sheets not an acceptable size. Fig(s) ___
5. MARGINS. 37 CFR 1.84(g): Acceptable margins:
   Top 2.5 cm Left 2.5cm Right 1.5 cm Bottom 1.0 cm
   SIZE: A4 Size
   Top 2.5 cm Left 2.5 cm Right 1.5 cm Bottom 1.0 cm
   SIZE: 8 1/2 x 11   3,4-6,8B,15
   Margins not acceptable. Fig(s) 3,4-6,8B,15
   ___ Top (T) ✓ ___ Left (L) ✓
   ___ Right (R) ___ Bottom (B)
6. VIEWS. 37 CFR 1.84(h)
   REMINDER: Specification may require revision to correspond to drawing changes.
   Partial views. 37 CFR 1.84(h)(2)
   ___ Brackets needed to show figure as one entity.
   Fig(s) ___
   ___ Views not labeled separately or properly.
   Fig(s) ___
   ___ Enlarged view not labeled separately or properly.
   Fig(s) ___
7. SECTIONAL VIEWS. 37 CFR 1.84 (h)(3)
   ___ Hatching not indicated for sectional portions of an object.
   Fig(s) ___
   ___ Sectional designation should be noted with Arabic or Roman numbers. Fig(s) ___

8. ARRANGEMENT OF VIEWS. 37 CFR 1.84(i)
   ___ Words do not appear on a horizontal, left-to-right fashion when page is either upright or turned so that the top becomes the right side, except for graphs. Fig(s) ___
9. SCALE. 37 CFR 1.84(k)
   ___ Scale not large enough to show mechanism without crowding when drawing is reduced in size to two-thirds in reproduction.
   Fig(s) ___
10. CHARACTER OF LINES, NUMBERS, & LETTERS.
   37 CFR 1.84(l)
   ✓ Lines, numbers & letters not uniformly thick and well defined, clean, durable, and black (poor line quality).
   Fig(s) ___
11. SHADING. 37 CFR 1.84(m)
   ___ Solid black areas pale. Fig(s) ___
   ___ Solid black shading not permitted. Fig(s) ___
   ___ Shade lines, pale, rough and blurred. Fig(s) ___
12. NUMBERS, LETTERS, & REFERENCE CHARACTERS.
   37 CFR 1.84(p)
   ___ Numbers and reference characters not plain and legible.
   Fig(s) ___
   ___ Figure legends are poor. Fig(s) ___
   ___ Numbers and reference characters not oriented in the same direction as the view. 37 CFR 1.84(p)(1)
   Fig(s) ___
   ___ English alphabet not used. 37 CFR 1.84(p)(2)
   Fig ___
   ___ Numbers, letters and reference characters must be at least .32 cm (1/8 inch) in height. 37 CFR 1.84(p)(3)
   Fig(s) ___
13. LEAD LINES. 37 CFR 1.84(q)
   ___ Lead lines cross each other. Fig(s) ___
   ___ Lead lines missing. Fig(s) ___
14. NUMBERING OF SHEETS OF DRAWINGS. 37 CFR 1.84(t)
   ___ Sheets not numbered consecutively, and in Arabic numerals beginning with number 1. Sheet(s) ___
15. NUMBERING OF VIEWS. 37 CFR 1.84(u)
   ___ Views not numbered consecutively, and in Arabic numerals, beginning with number 1. Fig(s) ___
16. CORRECTIONS. 37 CFR 1.84(w)
   ___ Corrections not made from prior PTO-948 dated ___
17. DESIGN DRAWINGS. 37 CFR 1.152
   ___ Surface shading shown not appropriate. Fig(s) ___
   ___ Solid black shading not used for color contrast.
   Fig(s) ___

COMMENTS

REVIEWER _____ WS _____ DATE 3/28/00 _____ TELEPHONE NO. 7033058404

ATTACHMENT TO PAPER NO. 4

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
(Case No. P043D2C3C)

In the Application of:

FARMWALD et al.

Serial No: 09/492,982

Filed: JANUARY 27, 2000

Title: METHOD OF OPERATING A MEMORY DEVICE HAVING A VARIABLE DATA INPUT LENGTH

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Group
Art Unit: 2818

Before
Examiner: T. Nguyen

Assistant Commissioner for Patents
Washington, DC 20231

RECEIVED

INFORMATION DISCLOSURE STATEMENT   JUN 0 6 2000

TECHNOLOGY CENTER 2800

Dear Sir:

In compliance with the duty of disclosure set forth in 37 C.F.R. §1.56, submitted herewith is a modified Form PTO-1449, including a copy of all of the documents listed therein. In accordance with 37 C.F.R. §1.97(c), the fee set forth in 37 C.F.R. §1.17(p) accompanies this statement.

Several of the documents listed in the PTO-1449 have been recently identified by a respondent in a pending ITC investigation, namely in re U.S. International Trade Commission Investigation No. 337-TA-431, Rambus Inc. vs Hitachi Ltd., et al., as prior art against the inventions claimed in the parent patent (i.e., U.S. Patent 6,034,918) of the instant application. An explicit reference to these documents is made in paragraph 17 on page 28, as well as in Exhibit A, of the

06/07/2000 SBUOHG   00000023 500998   09492982
03 FC:126   240.00 CH

Page -1-

RESPONSE OF HITACHI LTD. TO THE COMPLAINT AND NOTICE OF INVESTIGATION (hereinafter the "RESPONSE"). A copy of the RESPONSE is also submitted herewith.

It is respectfully requested that the Examiner make his consideration of these references formally of record with the next Office Action.

Respectfully submitted,

Date: June 2, 2000

Neil A. Steinberg
Reg. No. 34,735
650-944-7772

Page -2-

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
(Case No. P043D2C3C)

In the Application of:)
)
FARMWALD et al.   )
) **Group**
Serial No: 09/492,982) **Art Unit:** 2818
)
Filed: JANUARY 27, 2000) **Before**
) **Examiner:** T. Nguyen
Title: METHOD OF OPERATING A MEMORY)
  DEVICE HAVING A VARIABLE DATA)
  INPUT LENGTH   )

Assistant Commissioner for Patents
Washington, DC 20231

INFORMATION DISCLOSURE STATEMENT

Dear Sir:

In compliance with the duty of disclosure set forth in 37 C.F.R.
§1.56, submitted herewith is a modified Form PTO-1449, including a copy
of all of the documents listed therein. In accordance with 37 C.F.R.
§1.97(c), the fee set forth in 37 C.F.R. §1.17(p) accompanies this
statement.

Several of the documents listed in the PTO-1449 have been recently
identified by a respondent in a pending ITC investigation, namely in re
U.S. International Trade Commission Investigation No. 337-TA-431,
Rambus Inc. vs Hitachi Ltd., et al., as prior art against the
inventions claimed in the parent patent (i.e., U.S. Patent 6,034,918)
of the instant application. An explicit reference to these documents
is made in paragraph 17 on page 28, as well as in Exhibit A, of the

Page -1-

RESPONSE OF HITACHI LTD. TO THE COMPLAINT AND NOTICE OF INVESTIGATION
(hereinafter the "RESPONSE"). A copy of the RESPONSE is also submitted
herewith.

It is respectfully requested that the Examiner make his
consideration of these references formally of record with the next
Office Action.

Respectfully submitted,

Date: June 2, 2000

Neil A. Steinberg
Reg. No. 34,735
650-944-7772

PTO-1449 (Modified) 6	ATTY. DOCKET NO. P043D2C3C	SERIAL NUMBER 09/492,982
U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	APPLICANT(S) FARMWALD ET AL.	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	FILING DATE JANUARY 27, 2000	GROUP ART UNIT 2818

OIPE JUN 05 2000 PATENT & TRADEMARK OFFICE

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
TNT	4,330,852	May 18, 1982	Redwine et al.	365	221	
	4,703,418	Oct. 27, 1987	James	364	200	
	4,726,021	Feb. 16, 1988	Horiguchi et al.	371	38	
TNT	4,870,562	Sept 26, 1989	Kimoto et al.	364	200	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO	
TNT	S56-82961	July 7, 1981	Japan			YES	
	S57-14922	Jan. 26, 1982	Japan			YES	
	Sho 60-80193	May 8, 1983	Japan			YES	
	Sho 60-55459	Mar. 30, 1985	Japan			YES	
	S61-72350	April 14, 1986	Japan			YES	
	S63-142445	June 14, 1988	Japan			YES	
	B63-46864	Sept. 19, 1988	Japan			YES	
TNT	S64-29951	Jan. 31, 1989	Japan			YES	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

TNT	Watanabe, T.; "Session XIX: High Density SRAMS", IEEE International Solid State Circuits Conference pp. 266-267 (1987)
TNT	Ohno, C.; "Self-Timed RAM: STRAM", Fujitsu Sci. TechJ., 24, 4, pp 293-300 (Dec. 1988)
TNT	"Fast Packet Bus for Microprocessor Systems with Caches", IBM Technical Disclosure Bulletin, pp.279-282 (Jan 1989)
TNT	Gustavson, D. "Scalable Coherent Interface"; Invited Paper, COMPCON Spring '89, San Francisco, CA; IEEE, pp. 536-538 (Feb 27-Mar 3, 1989)
TNT	James, D.; "Scalable I/O Architecture for Busses"; IEEE, pp. 539-544 (April 1989)

EXAMINER TAN T. NGUYEN	DATE CONSIDERED 07/31/00

EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant.

PTO-1449 (Modified)	ATTY. DOCKET NO. P043D2C3C	SERIAL NUMBER 09/492,982
U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	APPLICANT(S) FARMWALD ET AL	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	FILING DATE JANUARY 27, 2000	GROUP ART UNIT 2818

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
TNT	4,205,373	May 27, 1980	Shah et al.	710	128	
TNT	4,845,670	Jul. 4, 1989	Nishimoto et al.	365	78	
	4,509,142	Apr. 2, 1985	Childers	364	900	
	4,183,095	Jan. 8, 1980	Ward	365	189.02	
TNT	4,685,088	Aug. 4, 1987	Iannucci	365	194	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO
TNT	0 246 767	April 28, 1987	EPO			
TNT	0 334 552	Mar. 16, 1989	EPO			
TNT	0 276 871	Jan. 29, 1988	EPO			

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

TNT	European Search Report for EPO Patent Application No. 00 101 1832
TNT	European Search Report for EPO Patent Application No. 89 30 2613
TNT	Z. Amital, "New System Architectures for DRAM Control and Error Correction", Monolithic Memories Inc., Electro/87 and Mini/Micro Northeast: Focusing on the OEM Conference Record, pp. 1132/4/31-?, (April 1987)
TNT	N. Siddique, "100-MHz DRAM Controller Sparks Multiprocessor Designs", Electronic Design, pp. 138-141, (Sept 1986)
TNT	H. Kuriyama et al., "A 4-Mbit CMOS SRAM WITH 8-NS SERIAL ACCESS TIME", IEEE Symposium On VLSI Circuits Digest Of Technical Papers, pp. 51-52, (June 1990)
TNT	J. Chun et al., "A 1.2ns GaAs 4K Read Only Memory", IEEE Gallium Arsenide Integrated Circuit Symposium Technical Digest, pp. 83-85, (Nov. 1988)
TNT	A. Fielder et al., "A 3 NS 1K X 4 STATIC SELF-TIMED GaAs RAM", IEEE Gallium Arsenide Integrated Circuit Symposium Technical Digest, pp. 67-70, (Nov. 1988)
TNT	JEDEC Standard No. 21C

EXAMINER TAN T. NGUYEN	DATE CONSIDERED 07/31/00

EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant.

UNITED STATES INTERNATIONAL TRADE COMMISSION
WASHINGTON, D.C.

Before The Honorable Debra Morriss
Administrative Law Judge

In the Matter of:	)
	)
	) Investigation No. 337-TA- 431
CERTAIN SYNCHRONOUS DYNAMIC	)
RANDOM ACCESS MEMORY DEVICES,	)
MICROPROCESSORS, AND PRODUCTS	)
CONTAINING SAME	)
	)

RESPONSE OF HITACHI, LTD. TO THE COMPLAINT
AND NOTICE OF INVESTIGATION

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RESPONSE TO THE COMPLAINT

Respondent Hitachi, Ltd. ("Hitachi") submits its Response to the Complaint, the letters amending the Complaint and the Notice of Investigation as follows.

Hitachi states that it has not yet had sufficient time and opportunity to collect and review all of the information that may be relevant to the matters raised herein and furthermore that discovery of Complainant and third parties has only just begun. Accordingly, Hitachi reserves the right to take further positions and raise additional defenses subsequent to the filing of this Response.

I.   INTRODUCTION

1.1.   Hitachi admits that Rambus Inc. ("Rambus") has requested the U.S. International Trade Commission to commence an investigation pursuant to section 337 of the Tariff Act of 1930, 19 U.S.C. § 1337 (a)(1)(B)(i), and that Rambus has requested remedies under the statute. Hitachi denies any unlawful conduct, and denies that either the action or any remedy is warranted. Except as expressly admitted herein, the allegations contained in paragraph 1.1 are denied.

1.2.   Hitachi denies the allegations contained in paragraph 1.2.

1.3.   Paragraph 1.3 was amended by Rambus' letter of April 4, 2000 and Hitachi's answer is to the paragraph as amended. Hitachi admits the allegations contained in the first sentence of paragraph 1.3. Hitachi admits that the '918 and '195 patents identify Rambus as "assignee." Hitachi lacks sufficient information to form a belief as to the truth or falsity of paragraph 1.3's allegation that Rambus "owns by assignment the entire right, title and interest in and to these

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patents," and therefore denies those allegations. Hitachi admits that Exhibits 3 and 4 contain certified copies of recorded assignments of an application filed April 18, 1990 for "Integrated Circuit I/O Using a High Performance Bus Interface." Hitachi states that the legal effect of such assignments on the '918 and '195 patents is a matter of law for the Commission. Except as expressly admitted herein, the allegations contained in paragraph 1.3 are denied.

      1.4.   Hitachi denies the allegations contained in paragraph 1.4.

      1.5.   Hitachi admits that Rambus seeks the relief described in paragraph 1.5, but denies that such relief is warranted. Hitachi denies the remaining allegations of paragraph 1.5.

II.   COMPLAINANT

      2.1.   On information and belief, Hitachi admits the allegations contained in paragraph 2.1.

      2.2.   Hitachi admits the allegations contained in the first sentence of paragraph 2.2. Hitachi lacks sufficient information to form a belief as to the truth or falsity of the allegations contained in the second and third sentences of paragraph 2.2, and therefore denies those allegations. Hitachi denies the allegations contained in the fourth sentence of paragraph 2.2.

      2.3.   Hitachi admits that attached as Exhibit 5 is a document that purports to be Rambus' annual report for 1999.

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III. PROPOSED RESPONDENTS

3.1.   Hitachi admits the allegations contained in the first sentence of paragraph 3.1. Hitachi admits that it is in the business of manufacturing and selling semiconductor devices, including SDRAMs and microprocessors, including products bearing the numbers identified in paragraphs 4.2 and 4.3 of the Complaint.[1] Hitachi further admits that it sells SDRAMs and microprocessors for importation into the United States. Hitachi admits that it sells certain SH-4 microprocessors to Sega Enterprises, Ltd. for incorporation into Sega's Dreamcast video game consoles. Except as expressly admitted herein, the allegations contained in paragraph 3.1 are denied.

3.2.   Hitachi admits the allegations contained in the first sentence of paragraph 3.2; and admits that Hitachi Semiconductor (America) Inc. ("HSA") is a subsidiary of Hitachi America, Ltd. and is in the business of importing into and selling in the United States Hitachi SDRAM devices and microprocessors. Hitachi denies the allegations contained in the third sentence of paragraph 3.2. Except as expressly admitted herein, the allegations contained in paragraph 3.2 are denied.

3.3.   Hitachi admits that Rambus and Hitachi, Ltd. entered into a semiconductor technology license agreement on October 30, 1992, and certain amendments and addenda thereto, including a royalty agreement, dated February 8, 1995, June 28, 1996, April 27, 1998, June 1, 1998 and November 12,

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[1]   Hitachi denies the allegations contained in the first and second sentences of footnote 1. Hitachi lacks sufficient information to form a belief as to the truth or falsity of the allegations contained in the third sentence of footnote 1.

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1998. Hitachi admits that copies of the license agreement, its amendments, and a royalty agreement are attached as Confidential Exhibit 7, and Hitachi refers to those agreements for their complete and accurate contents. Except as expressly admitted herein, the allegations contained in paragraph 3.3 are denied.

3.4.   Hitachi admits that Sega Enterprises, Ltd. is a Japanese corporation; admits that Sega Enterprises, Ltd. manufactures and sells "Dreamcast" video game consoles; and admits that Dreamcast video game consoles contain Hitachi SH-4 microprocessors. Hitachi lacks sufficient information to form a belief as to the truth or falsity of the remaining allegations contained in paragraph 3.4, and therefore denies those allegations.

3.5.   On information and belief, Hitachi admits that Sega of America is a California corporation. Hitachi lacks sufficient information to form a belief as to the truth or falsity of the allegations contained in paragraph 3.5, and therefore denies those allegations.

IV.   THE PRODUCTS AT ISSUE

4.1.   Hitachi admits that the Notice of Investigation specifies that the investigation concerns "certain synchronous dynamic random access memory devices, microprocessors, or products containing the same," without information sufficient to form a belief as to the identity of each specific product accused of infringing each specific asserted claim, as well as Complainant's asserted construction of each allegedly infringed claim element, and therefore Hitachi denies those allegations. Except as expressly admitted herein, the allegations contained in paragraph 4.1 are denied.

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4.2.   Hitachi admits that this paragraph purports to give a general description of an SDRAM but denies that it is a complete description or definition, and reserves the right to more fully describe and define an SDRAM. Hitachi admits that Rambus has asserted the listed products are accused but denies that any of the listed products infringe the asserted patents. Hitachi denies that it produces products with the numbers HB54A329 and HB54A649. Except as expressly admitted herein, the allegations contained in paragraph 4.2 are denied.

4.3.   Hitachi admits that this paragraph purports to give a general description of a microprocessor but denies that it is a complete description or definition, and reserves the right to more fully describe and define a microprocessor. Hitachi denies the allegations contained in the third and fourth sentences of paragraph 4.3. Except as expressly admitted herein, the allegations contained in paragraph 4.3 are denied.

4.4.   Hitachi lacks sufficient information to form a belief as to the truth or falsity of the allegations contained in the first sentence of paragraph 4.4, and therefore denies those allegations. Hitachi admits the allegations contained in the second sentence of paragraph 4.4, and further admits that the HSA website mentions the Sega Dreamcast console. Except as expressly admitted herein, the allegations contained in paragraph 4.4 are denied.

V.   THE PATENTS-IN-SUIT

A.   The '918 Patent

1.   Identification of the Patent and Ownership by Rambus

5.1.   Hitachi admits that U.S. Patent No. 6,034,918 identifies Rambus as assignee, was issued on March 7, 2000, identifies Michael Farmwald and Mark Horowitz as inventors, and is entitled "Method of Operating a Memory Having a Variable Data Output Length and a Programmable Register." Except as expressly admitted herein, the allegations contained in paragraph 5.1 are denied.

5.2.   On information and belief, Hitachi admits the allegations contained in paragraph 5.2.

2.   Non-Technical Description of the Patented Invention

5.3.   Hitachi denies that paragraph 5.3 provides an accurate description of the contents of the '918 patent and Hitachi refers to that patent for its complete and accurate contents. Hitachi admits that this paragraph purports to give general descriptions regarding the relationship between DRAM devices and microprocessors but denies that they are complete descriptions, and reserves the right to more fully describe the relationship between DRAM devices and microprocessors. Except as expressly admitted herein, the allegations contained in paragraph 5.3 are denied.

5.4.   Hitachi denies that paragraph 5.4 provides an accurate description of the purported invention of the '918 patent or that the purported invention of the '918 patent achieves the advantages described. Hitachi lacks

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sufficient information to form a belief as to the truth or falsity of the remaining allegations contained in paragraph 5.4, and therefore denies those allegations.

5.5. Hitachi denies that paragraph 5.5 provides an accurate description of the contents of the '918 patent and refers to that patent for its complete and accurate contents. Hitachi denies that any Hitachi SDRAMs or microprocessors infringe claims of the '918 patent, and denies the remaining allegations contained in paragraph 5.5.

3. Foreign Counterparts to the '918 Patent

5.6. Paragraph 5.6 was amended by Rambus' letter of April 12, 2000 and Hitachi's answer is to the paragraph as amended. Hitachi admits that Exhibits 10 and 11 are charts that purport to list each foreign patent issued that corresponds to the '918 patent and other information, but Hitachi lacks sufficient information to form a belief as to the truth or falsity of the allegations contained in Exhibits 10 and 11, or the letter of April 12, 2000 as it amends this paragraph, and therefore denies those allegations. Hitachi lacks sufficient information to form a belief as to the truth or falsity of the allegations contained in the third sentence of paragraph 5.6, and therefore denies those allegations; and further lacks sufficient information to form a belief as to the truth or falsity of Rambus' statement in its April 12, 2000 letter about the purported grant of a European patent, and therefore denies those allegations. Except as expressly admitted herein, the allegations contained in paragraph 5.6 are denied.

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B.   The '195 Patent

1.   Identification of the Patent and Ownership by Rambus

5.7.   Hitachi admits that U.S. Patent No. 6,038,195 identifies Rambus as assignee, was issued on March 14, 2000, identifies Michael Farmwald and Mark Horowitz as inventors, and is entitled "Synchronous Memory Device Having a Delay Time Register and Method of Operating Same." Except as expressly admitted herein, the allegations contained in paragraph 5.7 are denied.

5.8.   On information and belief, Hitachi admits the allegations contained in paragraph 5.8.

2.   Non-Technical Description of the Patented Invention

5.9.   Hitachi denies that paragraph 5.9 provides an accurate description of the '195 patent or that the purported invention of the '195 patent achieves the advantages described.

5.10.   Hitachi denies that paragraph 5.10 provides an accurate description of the contents of the '195 patent and refers to that patent for its complete and accurate contents. Hitachi denies that any Hitachi SDRAMs or microprocessors infringe claims of the '195 patent. Hitachi admits that this paragraph purports to give general descriptions regarding memory devices, but denies that they are complete descriptions, and reserves the right to more fully describe memory devices. Except as expressly admitted herein, the allegations contained in paragraph 5.10 are denied.

5.11.   Hitachi denies that paragraph 5.11 accurately describes the contents of the '195 patent and refers to that patent for its complete and accurate

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contents. Hitachi denies that any Hitachi SDRAMs or microprocessors infringe claims of the '195 patent.

5.12. Hitachi denies that paragraph 5.12 accurately describes the contents of the '195 patent and refers to that patent for its complete and accurate contents. Hitachi denies that any Hitachi SDRAMs or microprocessors infringe claims of the '195 patent.

5.13. Paragraph 5.13 was amended by Rambus' letter of April 12, 2000 and Hitachi's answer is to the paragraph as amended. Hitachi admits that Exhibits 12 and 13 are charts that purport to list each foreign patent issued that corresponds to the '195 patent and other information, but lacks sufficient information to form a belief as to the truth or falsity of the allegations contained in Exhibits 12 and 13 and Rambus' letter of April 12, 2000 as it amends this paragraph, and therefore denies those allegations. Hitachi lacks sufficient information to form a belief as to the truth or falsity of the allegations contained in the third sentence of paragraph 5.13; and further lacks sufficient information to form a belief as to the truth or falsity of Rambus' statement in its April 12, 2000 letter about the purported grant of a European patent, and therefore denies those allegations. Except as expressly admitted herein, the allegations contained in paragraph 5.13 are denied.

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VI. UNFAIR ACTS OF THE RESPONDENTS - PATENT INFRINGEMENT

6.1.   Hitachi denies the allegations contained in paragraph 6.1. Hitachi further denies the allegations contained in the subject heading preceding that paragraph.

6.2.   Hitachi admits that Exhibit 14 contains a Hitachi data sheet for SDRAMs HM5264165-B60, HM5264805-B60, and HM5264405-B60. Hitachi admits that Exhibit 15 purports to be a claim chart demonstrating how Rambus believes claim 1 of the '195 patent applies to the HM5264165-B60, HM5264805-B60 and HM5264405-B60 SDRAMs. Hitachi denies that the claim chart shows infringement and denies Complainant's alleged claim construction, including but not limited to all factual and legal conclusions as to validity, scope, meaning, or enforceability of the alleged '195 patent claims, as alleged in Exhibit 15. Hitachi further states that the meaning and effect of the claims and any limitations of the '195 patent is a matter of law for the Commission. Except as expressly admitted herein, the allegations contained in paragraph 6.2 are denied.

6.3.   Hitachi admits that Exhibit 16 purports to be a claim chart demonstrating how Rambus believes claim 18 of the '918 patent applies to the HM5264165-B60, HM5264805-B60 and HM5264405-B60 SDRAMs. Hitachi denies that the claim chart shows infringement and denies Complainant's alleged claim construction, including but not limited to all factual and legal conclusions as to validity, scope, meaning, or enforceability of the alleged '918 patent claims,

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as alleged in Exhibit 16. Hitachi further states that the meaning and effect of the claims and any limitations of the '918 patent is a matter of law for the Commission. Except as expressly admitted herein, the allegations contained in paragraph 6.3 are denied.

6.4.   Hitachi admits that Exhibit 17 and 18 contain a product brief and portions of a Hitachi hardware manual for the SH7750 microprocessor, which is part of the SH-4 series. Hitachi admits that Exhibit 19 purports to be a claim chart demonstrating how Rambus believes claim 23 of the '195 patent applies to the SH7750 microprocessor. Hitachi denies that the claim chart shows infringement and denies Complainant's alleged claim construction, including but not limited to all factual and legal conclusions as to validity, scope, meaning, or enforceability of the alleged '195 patent claims, as alleged in Exhibit 19. Hitachi further states that the meaning and effect of the claims and any limitations of the '195 patent is a matter of law for the Commission. Except as expressly admitted herein, the allegations contained in paragraph 6.4 are denied.

6.5.   Hitachi admits that Exhibit 20 purports to be a claim chart demonstrating how claim 1 of the '918 patent applies to the SH7750 microprocessor. Hitachi denies that the claim chart shows infringement and denies Complainant's alleged claim construction, including but not limited to all factual and legal conclusions as to validity, scope, meaning, or enforceability of the alleged '918 patent claims, as alleged in Exhibit 20. Hitachi further states that the meaning and effect of the claims and any limitations of the '918 patent is a

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matter of law for the Commission. Except as expressly admitted herein, the allegations contained in paragraph 6.5 are denied.

6.6.   Hitachi denies the allegations contained in paragraph 6.6.

6.7.   Hitachi admits that it received a copy of the Complaint in this matter and thereby obtained knowledge of the claims asserted therein. Hitachi denies the remaining allegations contained in paragraph 6.7.

VII.   SPECIFIC INSTANCES OF UNFAIR IMPORTATION AND SALE

7.1.   Hitachi admits the allegations contained in the first sentence of paragraph 7.1. Hitachi lacks sufficient information to form a belief as to the truth or falsity of the allegations contained in the second sentence of paragraph 7.1, and therefore denies those allegations. Hitachi further denies that it has engaged in any acts of unfair importation and sale.

7.2.   Hitachi admits the allegations contained in the first and second sentences of paragraph 7.2. Hitachi admits that Exhibit 26 purports to be a copy of a receipt for the purchase of a Hitachi SDRAM in the United States. Hitachi admits that Exhibit 27 is a copy of HSA's web page, and refers to that exhibit for its complete and accurate contents. Except as expressly admitted herein, the allegations contained in paragraph 7.2 are denied.

7.3.   Hitachi lacks sufficient information to form a belief as to the truth or falsity of the allegations contained in the first sentence of paragraph 7.3, and therefore denies those allegations. Hitachi admits the microprocessor in the photograph appears to bear a country of origin marking of Japan. Hitachi lacks sufficient information to form a belief as to the truth or

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falsity of the remaining allegations contained in paragraph 7.3, and therefore

denies those allegations.

7.4.   Hitachi admits that Exhibit 29 purports to be a copy of a

receipt for the purchase of a Dreamcast video game console in the United States.

Hitachi admits that Exhibit 30 is a copy of HSA's web page and refers to that

exhibit for its complete and accurate contents.

7.5.   Hitachi lacks sufficient information to form a belief as to

the truth or falsity of the allegations contained in the first sentence of

paragraph 7.5, and therefore denies those allegations. Hitachi admits that

Exhibit 31 purports to be a copy of a receipt for the purchase of a Dreamcast

video game console in the United States, and that it is dated March 19, 2000.

7.6.   Hitachi admits that certain of the products that Rambus has

accused enter the United States under Harmonized Tariff Schedule number

8542.13.80. Hitachi lacks sufficient information to form a belief as to the truth or

falsity of the remaining allegations contained in paragraph 7.6, and therefore

denies those allegations.

VIII. LICENSES

8.1.   Hitachi admits that Rambus licenses Rambus patents.

Hitachi denies Rambus' characterization of its license restrictions as "field of use"

restrictions and further states that the legal effect of the license restrictions under

the patent or antitrust laws is a matter of law for the Commission. Hitachi lacks

sufficient information to form a belief as to the truth or falsity of the allegations

contained in the first, second, third and fourth sentences of paragraph 8.1; and in

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particular lacks sufficient information to form a belief as to the truth or falsity of Rambus' allegations so far as they relate to the licensing of the '918 and '195 patents, and therefore denies those allegations. Hitachi admits that copies of the license agreements between Hitachi and Rambus accompany the Complaint as Confidential Exhibit 7, and Hitachi refers to those agreements for their complete and accurate contents. Except as expressly admitted herein, the allegations contained in paragraph 8.1 are denied.

IX. THE DOMESTIC INDUSTRY

9.1. Hitachi lacks sufficient information to form a belief as to the truth or falsity of the allegations contained in paragraph 9.1, and therefore denies those allegations.

9.2. Hitachi admits that Rambus licenses Rambus patents to companies that agree to manufacture RDRAM-compatible products. To the extent that the allegations contained in the second, third and fourth sentences of paragraph 9.2 refer to the license agreements between Hitachi and Rambus, Hitachi states that copies of the license agreements between Hitachi and Rambus accompany the Complaint as Confidential Exhibit 7, and Hitachi refers to those agreements for their complete and accurate contents. Hitachi lacks sufficient information to form a belief as to the truth or falsity of the remaining allegations contained in paragraph 9.2, and therefore denies those allegations.

9.3. Hitachi lacks sufficient information to form a belief as to the truth or falsity of the allegations contained in paragraph 9.3, and therefore

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denies those allegations. Hitachi denies that Rambus' alleged investments constitute a domestic industry.

9.4. Hitachi lacks sufficient information to form a belief as to the truth or falsity of the allegations in paragraph 9.4, and therefore denies those allegations.

9.5. Hitachi admits that Confidential Exhibit 32 purports to describe Rambus' investments in promoting its technology to potential licensees and other information, but Hitachi lacks sufficient information to form a belief as to the truth or falsity of the allegations contained in Exhibit 32, and therefore denies those allegations. Hitachi lacks sufficient information to form a belief as to the truth or falsity of the remaining allegations in paragraph 9.5, and therefore denies those allegations.

9.6. Hitachi lacks sufficient information to form a belief as to the truth or falsity of the allegations in the first sentence of paragraph 9.6, and therefore denies those allegations. Hitachi further states that copies of the license agreements between Hitachi and Rambus accompany the complaint as Confidential Exhibit 7, and Hitachi refers to those agreements for their complete and accurate contents. Hitachi admits the allegations contained in the second sentence of paragraph 9.6.

9.7. Hitachi lacks sufficient information to form a belief as to the truth or falsity of the allegations in paragraph 9.7, and therefore denies those allegations.

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9.8.   Hitachi states that the Rambus-Hitachi license agreement accompanies the Complaint as Confidential Exhibit 7, and Hitachi refers to those agreements for their complete and accurate contents. Hitachi lacks sufficient information to form a belief as to the truth or falsity of the remaining allegations in paragraph 9.8, and therefore denies those allegations.

9.9.   Hitachi lacks sufficient information to form a belief as to the truth or falsity of the allegations contained in paragraph 9.9, and therefore denies those allegations. Hitachi denies that Rambus' alleged investments constitute a domestic industry.

9.10.   Hitachi admits that Confidential Exhibit 32 purports to describe the number of Rambus employees specifically devoted to licensing the class of accused products under these patents, and Rambus' personnel and overhead expenses devoted to licensing the accused class of products. Hitachi lacks sufficient information to form a belief as to the truth or falsity of the allegations contained in Confidential Exhibit 32, and in Paragraph 9.10, and therefore denies those allegations.

9.11.   Hitachi lacks sufficient information to form a belief as to the truth or falsity of the allegations in paragraph 9.11, and therefore denies those allegations. Hitachi admits that Confidential Exhibit 32 purports to describe the number of Rambus employees that Rambus expects to devote to the licensing of the accused product throughout FY 2000 and 2001 and other information, but Hitachi lacks sufficient information to form a belief as to the truth or falsity of the

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information contained in Confidential Exhibit 32, and therefore denies those allegations.

X.   RELATED LITIGATION

10.1.   Paragraph 10.1 was amended by Rambus' letter of April 12, 2000 and Hitachi's answer is to the paragraph as amended. Hitachi admits that Rambus has sued Hitachi Europe GmbH in Germany for infringement of a European Patent and a German utility model. Hitachi further admits that Rambus filed Complaints against Hitachi, Ltd. and HSA in the United States District Court for the District of Delaware, asserting infringement of patents that are part of the same related family of patents as the '195 and '918 patents. Hitachi states that these actions have been transferred to the Northern District of California. Hitachi further states that Rambus' claims against Hitachi in the foregoing actions are wholly without merit. Except as expressly admitted herein, the allegations contained in paragraph 10.1 are denied.

XI.   RELIEF REQUESTED

11.1   Hitachi admits that Rambus is seeking the relief requested in paragraph 11.1, but denies that any such relief is warranted.

RESPONSE TO ALLEGATIONS CONTAINED IN RAMBUS' LETTER OF APRIL 4, 2000

The complaint has been amended by Rambus' letter of April 4, 2000, in which Rambus responded to certain inquiries by OUII concerning the complaint. Hitachi answers these allegations of the April 4, 2000 letter as follows:

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1.   Hitachi denies that Hitachi microprocessors practice any
claimed methods in the '918 and '195 patents. Hitachi lacks sufficient
information to form a belief as to the truth or falsity of the remaining allegations
of point 1 on page 2 of the April 4, 2000 letter, and therefore denies those
allegations.

2.   . Hitachi lacks sufficient information to form a belief as to
the truth or falsity of the allegations contained in the first sentence of point 2 on
page 2 of the April 4, 2000 letter, and therefore denies those allegations. Hitachi
admits that the HSA website mentions the Sega Dreamcast video game console,
admits that it markets its microprocessors for data processing, communications,
industrial, transportation and consumer applications, and further admits that it
markets its SDRAM devices for computer, workstation, and server applications.
Hitachi lacks sufficient information to form a belief as to the truth or falsity of the
remaining allegations contained in point 2, and therefore denies those allegations.

3.   Hitachi lacks sufficient information to form a belief as to
the truth or falsity of the allegations concerning Rambus' licensing activities
contained in point 3 on pages 2 and 3 of the April 4, 2000 letter, and therefore
denies those allegations. To the extent that such allegations refer specifically to
the License Agreement between Hitachi and Rambus, Hitachi admits that copies
of the license agreements between Hitachi and Rambus accompany the Complaint
as Exhibit 7, and Hitachi refers to those agreements for their complete and
accurate contents. Hitachi denies that Rambus' alleged licensing activities
constitute a domestic industry. Hitachi admits that Confidential Exhibit 32

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purports to set forth Rambus' alleged investments in licensing technology other than RDRAM technology under the '918 and '195 patents. Hitachi lacks sufficient information to form a belief as to the truth or falsity of the information set forth in Confidential Exhibit 32, and therefore denies those allegations. Except as expressly admitted herein, Hitachi denies each of the allegations of point 3 on pages 2 and 3 of the April 4, 2000 letter.

    4.   Hitachi lacks sufficient information to form a belief as to the truth or falsity of the allegations contained in point 4 on page 3 of the April 4, 2000 letter, and therefore denies those allegations.

    Rambus' letter of April 12, 2000 amends paragraphs of the Complaint and Hitachi has answered the allegations contained in those paragraphs as amended by the April 12, 2000 letter. Except as expressly admitted herein, Hitachi denies the allegations contained in Rambus' letters of April 4, 2000 and April 12, 2000.

RESPONSE TO NOTICE OF INVESTIGATION

    Hitachi admits that the notice of investigation names Hitachi, Ltd. and Hitachi Semiconductor (America) Inc., as respondents but denies that either has violated 19 U.S.C.§ 1337 by importing into the United States, selling for importation into the United States, or selling within the United States after importation certain synchronous dynamic random access memory devices, microprocessors, or products containing same by reason of infringement of claims 1-24, 27, 32, and 33-39 of U.S. Letters Patent 6,038,195 or claims 1-3, 6-10, 13-16, 18-21, 24-26, 29-31, 33-34 and 37-38 of U.S. Letters Patent 6,034,918.

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Hitachi denies that the Commission should issue a permanent exclusion order, a permanent cease and desist order, or any other relief. Except as expressly admitted herein, Hitachi denies the allegations contained in the Notice of Investigation.

INFORMATION UNDER COMMISSION RULE 210.13

1.   Hitachi states that it is still attempting to determine the quantity and value of imports of the several accused articles.

2.   Hitachi states that the United States is significant to its operations. Hitachi further states that its worldwide production capacity and sales for SDRAMs and SH microprocessors is as set forth in Confidential Exhibit B.

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AFFIRMATIVE DEFENSES

Hitachi asserts the following affirmative and other defenses and reserves the right to modify and expand the defenses as discovery proceeds in this investigation.

Facts Giving Rise To The Affirmative Defenses

1.   The '195 patent issued from an application filed November 20, 1998. Rambus filed a continuation application of the '195 patent on November 19, 1999 which issued as the '918 patent. Each of these applications asserts that it is a continuation and/or division of earlier-filed applications in a chain of related applications leading back to an original parent application filed April 18, 1990. Rambus abandoned the original parent application in favor of at least 11 applications filed in 1992 each of which was asserted to be a continuation or division of the parent application. Thereafter, Rambus filed additional continuations and divisions also claiming the benefit of the April 18, 1990 parent application. A total of at least 41 applications were filed in the United States as continuation or divisional applications which assert the benefit of the common April 18, 1990 filing date (collectively, the "Related Family"). These related applications resulted in at least 25 issued patents, including the '195 and '918 patents.

2.   The parent application filed April 18, 1990 contained claims 1-150. In filing the continuation and division applications in the Related Family, Rambus adopted a practice of filing a Preliminary Amendment which cancelled the original claims and added various new claims. Beginning about

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1994, the Preliminary Amendment would be accompanied by a Request To Approve Drawing Changes, which would amend various figures of the original disclosure and/or add new figures. In these amendments to the claims and the drawings, Rambus would assert that the changes were supported by the original specification filed April 18, 1990. Some of these same amendments to the drawings and specification, as well as other amendments to the drawings and specification, were made to other applications in the Related Family.

3.   The '195 patent as issued contains 40 claims, and the '918 patent as issued includes 38 claims. These claims contain numerous elements which have the same or closely related language to issued claims in numerous patents in the Related Family. By way of example, claim 1 of the '918 patent is substantially similar to claim 1 of Patent 6,032,214, which is part of the Related Family. Statements in the file history of prosecution of applications in the Related Family which claim similar or the same subject matter, or which refer to similar or the same terms or phrases, and assertions to the Examiner and Patent Office concerning the meaning and scope of such subject matter or terms or phrases, are applicable to and/or constitute admissions concerning the scope and support of corresponding claim language in the '918 and '195 patents.

4.   After filing the parent application on April 18, 1990, Rambus licensed the technology to various third parties who were to manufacture Rambus-compatible memory devices under the trademark "RDRAM." Rambus licensed a variation of the original disclosure which was called the "Base" technology. This was later revised to create a "Concurrent" technology, which in

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turn was further revised to create a "Direct" technology. With each revision of the

RDRAM technology, from "Base" to "Concurrent" to "Direct", the technology

was changed in significant aspects from the disclosure of the April 18, 1990

parent application. Numerous aspects of the original disclosure were abandoned,

and certain other aspects and circuitry were substantially changed. On

information and belief, various changes to the Base, Concurrent, and Direct

versions of the RDRAM technology were the development of third parties and/or

persons different than the named inventors of the '195 and '918 patents.

       5.   Prior to April 18, 1990, the named inventors attended

meetings and/or received mailings of an IEEE subgroup working on various

standards for semiconductor memories, and in particular attended a subgroup

known as the Scalable Coherent Interface or SCI. The SCI group considered

various memory issues, such as inefficiency caused by latency, and studied

various solutions. The group later evolved into a related group called RamLink.

The SCI and RamLink groups were part of various standard-setting activities from

the late 1980s and into the mid-1990s, which included standard development

efforts such as SyncLink. The named inventors of the '195 and '918 patents, and

various employees of Rambus, attended numerous of these standard-setting

meetings, and/or received minutes and reports from these meetings, from the late

1980s the mid-1990s.

       6.   Another standard-setting activity involving synchronous

DRAMs involved certain committees of the Joint Electronic Devices Engineering

Council ("JEDEC"), including but not limited to the JC-42.3 committee on RAM

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memories. In 1991, JEDEC members began considering the development of standards for synchronous DRAM (SDRAM) technology. Rambus began attending JEDEC committee meetings no later than December 1991 and formally joined as a committee member at least as early as 1992. Rambus continued as a committee member until it announced it was leaving JEDEC by a June 17, 1996 letter.

       7.   During prosecution of the Related Family, including but not limited to the '195 and '918 patents, the claims of the applications were amended to cover the evolving Base/Concurrent/Direct Rambus technology and/or the synchronous DRAM standards developed in SCI, RamLink, and JEDEC, even though the parent application lacked support for the belatedly-claimed features and the later technology was not the invention of the named inventors. Also, Rambus through its attorneys made contradictory assertions in different applications of the Related Family, in order to obtain allowance of the claims in those applications and without calling attention that its statements were contrary to statements in other applications containing the same claim language. The purpose of this pattern of conduct was to obtain claim coverage on technology which was altered from and not the invention of the named inventors in the parent application, in order to improperly encompass these later developments.

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First Defense
(Invalidity)

8.   The allegations of paragraphs 1-7 are incorporated by reference in this First Defense.

9.   The '195 and '918 patents are invalid for failing to comply with the conditions and requirements for patentability set forth in the United States Patent Statute, including, but not limited to 35 U.S.C. §§ 101, 102, 103, 112, 113, 115, 120, 121 and 132.

10.   The issued claims of the '195 and '918 patents are not entitled to the benefit of the April 18, 1990 filing date of the parent application nor to the filing dates of certain other applications in the Related Family leading to the '195 and '918 patents.

11.   The '195 and '918 patents are invalid for failure to satisfy the requirements of 35 U.S.C. § 112. In view of the various amendments that occurred during the long prosecution history of the patents and earlier applications in the Related Family, the claims of the '195 and '918 patents as issued now bear little resemblance to the purported invention that was described in the original application. Numerous claim limitations do not have any support in the original specification. The asserted claims are invalid as inoperable. The asserted claims are invalid as not enabled. The asserted claims are invalid for failure to distinctly claim what the named inventors viewed as their invention. The asserted claims are invalid for omitting essential elements.

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12. During the prosecution of the applications in the Related Family, Rambus filed Requests to Approve Drawing Changes, which amended the figures in a manner unsupported by the original specification and was misleading as to the amended claims, in violation of 35 U.S.C. § 113.

13. The asserted claims of the '195 and '918 patents are invalid for presenting new matter and new claims which are unsupported by the oaths of the named inventors, in violation of 35 U.S.C. §§ 115 and 132.

14. On information and belief, the written description and the drawings are not in such full, clear, concise and exact terms as to enable any person skilled in the art to make and use the same without undue experimentation. On information and belief, the circuitry of various figures is inoperative, and/or cannot be used without undue experimentation. Such inoperativeness is evidenced by the abandonment of such structure in the Rambus Base/Concurrent/Direct RDRAM products.

15. The Patent Examiner who examined the original parent application asserted that Rambus had claimed eleven different alleged inventions in the 150 claims that were originally filed. The Examiner required Rambus to elect which group or groups of claims it wished to prosecute. Over the next decade and to the present day, Rambus has filed divisional and continuation applications in the Related Family, with similar and/or overlapping claims in the various related applications. Rambus has not maintained the line of demarcation that is required between the independent and distinct inventions that prompted the restriction requirement in the original application and that led to the multiple

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divisional applications, in violation of the principle of "consonance." Accordingly, the '195 and '918 patents are invalid.

16.   Moreover, due to the lack of consonance, the protections of 35 U.S.C. § 121 do not apply to the patents resulting from such divisional applications. Various of the Rambus Related Family, including the '195 and '918 patents, are therefore invalid for double patenting.

17.   The asserted claims of the '195 and '918 patents are invalid under 35 U.S.C. §§ 102 and/or 103. A listing of the printed prior art references which, either alone or in combination, render the '195 and/or '918 patents invalid is attached to this response as Exhibit A. In addition, the asserted claims are invalid for prior use and/or sale before the filing date of the '195 and '918 patents in the United States, its territories or possessions. Further, the printed prior art publications refer in part to certain standard-setting activities which constitute prior art, and/or concern certain products which were made, used or sold in the United States and which separately constitute prior art.

18.   Hitachi also believes that the asserted claims of the '195 and '918 patents are invalid due to their failure to satisfy other requirements of the patent statutes, and Hitachi reserves the right to alter or supplement its defense as the investigation proceeds.

Second Defense
(Noninfringement)

19.   The allegations of paragraphs 1-18 are incorporated by reference in this Second Defense.

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20.   Hitachi denies that the accused products, either literally or under the doctrine of equivalents, infringe the asserted claims of either the '195 or '918 patent. This affirmative defense is based upon Hitachi's current knowledge and understanding, and Hitachi reserves the right to present and rely on any and all support for this defense discovered in the course of this investigation. Hitachi will in the course of this investigation, *inter alia*, take discovery concerning Complainant's infringement contentions, including Complainant's contentions as to construction of the asserted claim elements, and will present Hitachi's contentions as to proper claim construction and non-infringement.

21.   The asserted claim language was added long after the original filing date in an attempt to improperly cover the Base/Concurrent/Direct Rambus technology and/or synchronous DRAM technology pursuant to the JEDEC standards. The claim language is instead restricted in scope to the meanings in the original application as filed on April 18, 1990, when supported at all, and as properly construed does not cover the accused products. In addition, the accused products are so different in function and operation from that originally disclosed or properly claimed in the '195 and '918 patents that the accused products could not be found to infringe under a doctrine of equivalents analysis.

22.   The drawing amendments submitted after the filing date of the original application dated April 18, 1990 may not be used under 35 U.S.C. § 113 to supplement the original disclosure for the purpose of interpretation of the

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scope of any claim, and Rambus is improperly attempting to supplement the

original disclosure so as to encompass the accused devices.

23. Hitachi reserves the right to alter or supplement its non-infringement defense as the investigation proceeds.

Third Defense
(Inequitable Conduct and Patent Misuse)

24. The allegations of paragraphs 1-23 are incorporated by reference in this Third Defense.

25. Upon information and belief, the '195 and '918 patents are unenforceable and have been misused for reasons that include but are not limited to the facts set forth above. Rambus' conduct includes improper and knowing filing of amendments which added claims and drawings not supported in the original application, failure to disclose the derivation of the subject matter of the added claims, improper inventorship, misleading and inconsistent statements made in applications of the Related Family, and failure to maintain the proper line of demarcation between the divisional and continuation applications. Furthermore, the unenforceability of certain other patents in the Related Family taint the '195 and '918 patents and also render unenforceable the '195 and '918 patents.

26. On information and belief, Rambus engaged in a pattern of conduct to file and amend the applications in the Related Family, add new claims and new drawings, and make assertions to the Patent Office to attempt to encompass the features of the altered Rambus Base/Concurrent/Direct technology

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and/or the synchronous DRAM technology without regard to support or

inventorship and by making misleading and false statements to the U.S. Patent

Office. On information and belief, Rambus was aware that various language of

the claims as amended was unsupported or contrary to the original specification,

and such amendments were made with an intent to deceive and improperly

encompass synchronous DRAM technology covered by the JEDEC standards

and/or the Base/Concurrent/Direct Rambus technology which had changed from

the original disclosure on April 18, 1990.

27.   Rambus through its attorneys made contradictory assertions

in different applications of the Related Family, in order to obtain allowance of the

claims in those applications and without calling attention to the fact that its

statements were contrary to statements in other applications concerning the same

language. The purpose of this pattern of conduct was to obtain claim coverage on

technology which was not the invention of the named inventors and not

adequately disclosed in the April 18, 1990 parent application. Under the Doctrine

of Infectious Unenforceability, the improper conduct concerning any of the

patents and applications in the Related Family will taint and infect the

enforceability of the '195 and '918 patents.

28.   JEDEC Standards relating to SDRAMS have existed since

1992. Since 1992, several generations of JEDEC SDRAMs have been introduced.

JEDEC-compliant SDRAMs perform various functions which Rambus has

attempted to cover by claims filed belatedly and improperly in an attempt to cover

those functions despite lack of support in the original disclosure. Rambus' inventors and personnel connected with the prosecution of the '195 and '918 patents were during all relevant times aware of the 1992 and subsequent JEDEC SDRAM standards, having participated in the industry and the standard-setting process prior to all relevant times involving the pendency of the applications which issued as the '195 and '918 patents.

29.   Rambus' inventors and personnel connected with the prosecution of the '195 and '918 patents were not in possession of the inventions ultimately claimed in the '195 and '918 patents prior to those patents' actual filing dates in 1998 and 1999. Instead, Rambus' inventors and personnel connected with the prosecution of the '195 and '918 patents added claims to those patents to read on JEDEC-compliant SDRAMs.

30.   The Rambus named inventors and other Rambus personnel also participated in other industry standard-setting efforts in the late 1980s and early 1990s and improperly amended the applications in the Related Family to attempt to cover the technology developed through those efforts. On information and belief, the Rambus named inventors and/or their attorneys came into possession of the claims not through their own effort but by studying the standards developed by others and/or the changed Base/Concurrent/Direct technology as developed by others.

31.   Rambus' filing of new claims to read on JEDEC-compliant SDRAMs and the changed Base/Concurrent/Direct technology constituted

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material information which was false and misleading and constituted inequitable conduct. Moreover, such information is material to the patentability of the '195 and '918 patents under 37 CFR 1.56. On information and belief, Rambus knowingly failed to disclose this material information to the Patent Office during the prosecution of the '195 and '918 patents, and other applications in the Related Family, which constitutes inequitable conduct rendering all patents in the Related Family unenforceable.

32. Rambus' attempt to enforce patents acquired through misrepresentations and omissions also constitutes patent misuse and/or a violation of the antitrust laws. But for Rambus' knowing misrepresentations and omissions to the Patent Office, the '195 and '918 patents would not have issued. Rambus already controls the RDRAM technology which is the significant alternative architecture to the "open" JEDEC interface standard. If Rambus' patents are construed as covering the JEDEC standards governing SDRAMs, then Rambus has monopoly power or a dangerous probability of successfully monopolizing the relevant U.S. markets for the interface technology for high-speed synchronous DRAM memory, and for synchronous DRAM memory and logic chips which control such memory. On information and belief, Rambus made these misrepresentations and omissions with a specific intent to monopolize the relevant markets, and with the purpose and/or effect of restraining competition in the relevant markets.

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Fourth Defense

(Unclean Hands, Equitable Estoppel, Implied License, and Patent Misuse in Connection with Misconduct in Standard-Setting Activities and Other Conduct)

33. The allegations of paragraphs 1-32 are incorporated by reference in this Fourth Defense.

34. Rambus is asserting patents that are unenforceable due to Rambus' misuse and/or violation of the antitrust laws, including but not limited to Rambus' actions and concealment in connection with standard-setting activities and participation in standards-setting organizations. Because of this same conduct, Rambus comes to this proceeding with unclean hands and should be equitably estopped from obtaining any relief.

35. JEDEC is the semiconductor engineering standardization body of the Electronic Industries Alliance ("EIA"), a non-profit standard-setting organization open to the industry and designed to foster competition in the several markets for computer chips. In the 1990s, JEDEC coordinated the development of technology standards for synchronous DRAM, including standards for the synchronous DRAM "interfaces" between memory chips and logic chips at issue in this action. Synchronous DRAM products and interfaces conforming to the JEDEC standards are commonly called SDRAM.

36. Rambus was a JEDEC member at that time and knew or should have known of JEDEC's disclosure rules, designed so that no firm could secretly capture the open standard under development. These rules required Rambus to disclose to JEDEC the existence and nature of its patent rights and

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pending patent applications that could bear upon a standard that JEDEC members had under development. Upon disclosure, holders of patents or applications were to make their patents available without charge or under reasonable terms and conditions that were demonstrably free of any unfair discrimination. JEDEC members and participants had to rely on the good faith of their fellow JEDEC members and participants to comply with their duty to disclose if JEDEC members were to develop truly open standards, as was their charter.

37.   Instead of fulfilling its duty to disclose, Rambus concealed its patent position, including its then-pending patent applications that through subsequent applications led to the '195 and '918 patents. During JEDEC committee meetings, while Rambus remained silent about its patent applications, and its plan to file additional applications to attempt to cover the proposed standards, other JEDEC members and participants participated in good faith, and shared their technical information so that open industry standards could be developed. Rambus then improperly revised its pending applications and subsequent applications based on then-pending applications to cover what it learned from its participation in JEDEC and the disclosures of other JEDEC members and participants. Thus Rambus intentionally misled JEDEC members into promulgating a standard which, according to Rambus' allegations against Hitachi, is not the open standard the JEDEC members intended and believed it to be.

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38.   Without knowledge of Rambus' pending applications,
JEDEC determined an industry standard for SDRAM interface technology.
JEDEC members and participants reasonably and substantially relied on Rambus'
silence regarding its patent position and patent applications and, thus, continued to
participate in developing the JEDEC open standard instead of exploring
alternative standards. Hitachi and other firms in the industry spent millions of
dollars in product development, testing, and marketing of SDRAM chips and
other products compatible with what was thought to be an open technology.
Rambus now asserts that certain of its patents cover the JEDEC SDRAM interface
technology standards. Moreover, in suing Hitachi in successive lawsuits in
federal court, in making public comments, and in pursuing this action, Rambus
has sent a signal to Rambus' competitors and customers that if Rambus has its
way, there will be no competition in the relevant markets.

39.   Likewise, Rambus has engaged in anticompetitive licensing
and tying practices that preclude it from obtaining relief in this proceeding.
Rambus has licensed its technology both to DRAM manufacturers, including
Hitachi, Ltd., Samsung, NEC, and others, and to manufacturers of Logic Chips,
including Intel. Rambus' licenses and technical collaboration agreements impose
substantial and unwanted obligations on licensees. For example, Rambus'
licenses do not simply permit the use of Rambus patents. Rather, the license
agreements require, as a condition of licensing one of Rambus' patents, that the
licensees license numerous other Rambus patents. The license agreements also
require the licensees to use the patents to manufacture synchronous memory only

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to Rambus' requirements, including requiring the licensees to use Rambus-controlled tests and know-how to manufacture their products to Rambus' specifications.

40.   Rambus already controls the RDRAM standard which is the significant alternative architecture to the "open" JEDEC standard. If Rambus' patents are construed as covering the JEDEC standards governing SDRAMs, then Rambus has monopoly power or a dangerous probability of successfully monopolizing the relevant U.S. markets for the interface technology for high-speed synchronous DRAM memory, and for synchronous DRAM memory and logic chips.

Fifth Defense
(Non-Infringement/Implied License/Patent Exhaustion as to Hitachi Microprocessors)

41.   The allegations of paragraphs 1-40 are incorporated by reference in this Fifth Defense.

42.   The asserted claims of the '195 and '918 patents are directed to synchronous DRAM apparatus, methods of operating synchronous DRAMs, and methods of controlling synchronous DRAMs during operation. A synchronous DRAM is a critical element of each asserted claim. The '195 and '918 patents do not claim any type of controller in a microprocessor. Hitachi's accused SH microprocessors cannot, by itself, infringe any asserted claim of the '195 or '918 patent.

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43.   Hitachi's accused SH microprocessors are designed for use not only with synchronous DRAM but also with a variety of other types of DRAM memories, and as such is a staple article of commerce whose importation and sale cannot constitute unfair competition. Thus, an exclusion order directed to the SH is not an appropriate remedy.

44.   The SH as used in the Sega Dreamcast system together with synchronous DRAMs manufactured by third parties. To the extent such third-party synchronous DRAMs are or will be licensed by Rambus, Rambus has exhausted its patent rights and/or has granted an implied license to use the Hitachi SH microprocessors in combination with any licensed synchronous DRAM.

45.   Moreover, Rambus has excluded any third-party (i.e., non-Hitachi) synchronous DRAMs from this investigation, and thus cannot assert that any non-Hitachi synchronous DRAMs are critical components to establish infringement of the '195 and '918 Patents. Since a synchronous DRAM is a critical element of each of the asserted claims, but only third-party synchronous DRAMs which have not been accused of infringement are used in the Sega Dreamcast, Rambus cannot establish infringement of the accused SH microprocessors. Thus, an exclusion order directed against the SH microprocessors by itself, or against the Sega Dreamcast system, is not an appropriate remedy.

<u>Sixth Defense</u>
(Lack of Domestic Industry)

46.   Rambus has not adequately alleged and cannot prove the existence of a domestic industry or that a domestic industry is in the process of being established.

<u>REQUEST FOR RELIEF</u>

WHEREFORE, Hitachi, Ltd. respectfully requests that the Commission:

i.   Determine that Hitachi, Ltd. and HSA do not violate Section 337 of the Tariff Act of 1930 as amended (19 U.S.C. § 1337).

ii.   ˙Deny all relief requested in the Complaint.

iii.   Determine that the '918 and '195 patents are unenforceable and misused

iv.   Determine that the '918 and '195 patents are invalid and not infringed.

v.   Award Hitachi its full costs of this action, including reasonable attorneys' fees.

vi.   Order the investigation terminated.

Dated: May 19, 2000   Respectfully submitted,

                                            By: _____
                                            One of the Attorneys for
                                            Respondent Hitachi, Ltd.

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VERIFICATION OF RESPONSE

I, Seijio Shiraishi, being the Department Manager of the Strategic Business Planning Division, Semiconductor & Integrated Circuits, for Hitachi, Ltd., and as such I am authorized to make this verification on behalf of Hitachi, Ltd.   I further declare that the foregoing Response was prepared with the advice and assistance of counsel, and the information therein was gathered from a number of persons, none of whom possesses all the information set forth in the Response.   Based on the foregoing, and based on the information currently available to Hitachi, Ltd., I declare that to the best of my knowledge, information and belief that the foregoing responses are true and correct.

I declare under penalty of perjury of the laws of the United States of America that the foregoing is true and correct.

Executed on this __15__ day of May, 2000.

HITACHI. LTD.

Seijin Shiraishi

<u>CERTIFICATE OF SERVICE</u>

The undersigned hereby certifies that copies of the foregoing

**RESPONSE OF HITACHI, LTD. TO THE COMPLAINT
AND NOTICE OF INVESTIGATION**

were caused to be served today, May 19, 2000, on the following counsel of record by the manner indicated:

Donna R. Koehnke, Secretary U.S. International Trade Commission 500 E Street, S.W. Washington, D.C. 20436	(Original and 6 copies) (By hand)
The Honorable Debra Morriss Administrative Law Judge U.S. International Trade Commission 500 E Street, S.W., Room 317 Washington, D.C. 20436	(2 copies) (By hand)
Karin J. Norton, Esq. Office of Unfair Import Investigations U.S. International Trade Commission 500 E Street, S.W., Room 401-M Washington, D.C. 20436	(1 copy - By hand)
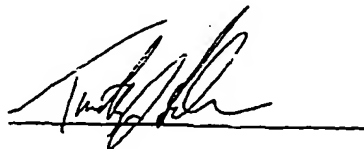
For Complainant Rambus Inc.:

Cecilia H. Gonzalez, Esq. HOWREY SIMON ARNOLD & WHITE, LLP 1299 Pennsylvania Ave., N.W. Washington, D.C. 20004	(1 copy - By hand)

For Respondent Sega of America, Inc.:

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WDC99 231551-1.017571.0403

Invalidating Prior Art to the '195 and '918 Patents

This appendix is based upon Hitachi's current factual knowledge and understanding.
Hitachi reserves the right to rely on and present additional invalidating prior art as to the '195
and '918 patents discovered in the course of this investigation.

1. Kawamasa, K.; "Memory Control Method"; Japanese Patent Application Kokai
   Publication No. S56-82961 (July 7, 1981).*

2. Taguri, J.; "Memory Storage Device"; Japanese Patent Application Kokai Publication No
   S57-14922 (January 26, 1982).*

3. Redwine et al.; "Semiconductor Read/Write Memory Array Having Serial Access";
   United States Patent No. 4,330,852 (May 18, 1982).

4. Hasegawa, J.; "Memory System"; Japanese Laid Open Patent Application No. Sho 60-
   80193 (May 8, 1983).*

5. Miyazaki, Y.; "Block Transfer and Storage Control Method"; Japanese Laid-open Patent
   Application Sho 60-55459 (March 30, 1985).*

6. Hashimoto, S.; "Data Transfer Control System"; Japanese Patent Application Kokai
   Publication No. S61-72350 (April 14, 1986).*

7. Fischer, M.; "Fair Arbitration Technique for a Split Transaction Bus in a Multiprocessor
   Computer System"; United States Patent No. 4,785,394 (November 15, 1988).

8. Wantanabe, T.; "Session XIX: High Density SRAMs"; IEEE International Solid State
   Circuits Conference pp. 266-267 (1987).

9. James, D.; "Method and Apparatus for Performing Variable Length Data Read
   Transactions"; United States Patent No. 4,703,418 (October 27, 1987).

10. Taguchi, Y.; "Memory Device"; Japanese Patent Application Kokai Publication No. S63-
    142445 (June 14, 1988).*

11. Taguri, J.; "Memory Storage Device"; Japanese Patent Application Kokoku Publication
    No. B63-46864 (September 19, 1988).*

12. Horiguchi et al., "Semiconductor memory having error correcting means", United States
    Patent No. 4,726,021 (February 16,1988).

13. Ohno, C.; "Self-Timed RAM: STRAM"; Fujitsu Sci. Tech J., 24, 4, pp.293-300 (Dec.
    1988).

14. Fast Packet Bus for Microprocessor Systems with Caches, IBM Technical Disclosure
    Bulletin, pp. 279-282 (January 1989).

15. Kumagai, T.; "Storage System"; Japanese Patent Application Kokai Publication No. S64-
    29951 (January 31, 1989).*

16. Gustavson, D.; "Scalable Coherent Interface"; Invited Paper, COMPCON Spring '89, San Francisco, CA; IEEE, pp. 536-538 (Feb. 27-Mar. 3, 1989).

17. James, D.; "Scalable I/O Architecture for Buses"; IEEE. pp. 539-544 (April 1989).

18. Kimoto et al., "Micro-computer Capable of Accessing Internal Memory at a Desired Variable Access Time"; U.S. Patent No. 4,870,562 (September 26, 1989).

19. JEDEC SDRAM standards.

* Translation Included

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
(Case No. P043D2C3C)

In the Application of:)
)
    FARMWALD et al.   )
)   Group
Serial No: 09/492,982   )   Art Unit: 2818
)
Filed: JANUARY 27, 2000   )   Before
)   Examiner: T. Nguyen
Title: METHOD OF OPERATING A MEMORY   )
        DEVICE HAVING A VARIABLE DATA   )
        INPUT LENGTH   )

Assistant Commissioner for Patents
Washington, DC 20231

AMENDMENT

Dear Sir:

In response to the Office Action dated May 19, 2000, kindly amend

the application as follows:

IN THE CLAIMS:

Kindly **amend** the following claims:

1   153. The method of claim 151 further including:

2   providing second block size information to the memory device,

3   wherein the second block size information defines a second amount of

4   data to be input by the memory device in response to a write request;

5   and

6   issuing a [the] second write request to the memory device, wherein

7   in response to the second write request, the memory device inputs the

8   second amount of data corresponding to the second block size

9   information.

155. The method of claim 151 further including providing the **first** amount of data corresponding to the first block size information to the memory device.

157. The method of claim 156 wherein the **first amount of** data is provided to the memory device after a delay time transpires.

161. A method of operation [of] in a synchronous memory device, wherein the memory device includes a plurality of memory cells, the method of operation of the memory device comprises:

receiving first block size information from a [bus] controller, wherein the first block size information defines a first amount of data to be input by the memory device in response to a write request;

receiving a first write request from the [bus] controller synchronously with respect to an external clock signal; and

inputting the first amount of data corresponding to the first block size information in response to the first write request.

162. The method of claim 161 wherein the **first amount of** data corresponding to the first block size information is sampled synchronously with respect to the external clock signal.

1   163. The method of claim 161 further including:

2   receiving second block size information, wherein the second block

3   size information defines a second amount of data to be input in

4   response to a [second] write request;

        receiving a second write request from the bus controller; and

6   inputting the second amount of data corresponding to the second

7   block size information, in response to the second write request.

---

1   174. The method of claim 171 wherein the [first] block size

2   information is a binary representation of the first amount of data to

3   be input in response to the first write request.

1   175. The method of claim 171 wherein the [first] block size

2   information is provided by a controller.

Kindly **ADD** the following claims:

1   176. The method of claim 161 wherein the first amount of data is

2   input, in response to receipt of the first write request, after a delay

3   time transpires.

1   177. The method of claim 176 wherein the delay time is

2   representative of a number of clock cycles of the external clock signal

3   that transpire before the first amount of data is input.

Page 3

REMARKS

This Amendment seeks to place this application in condition for allowance. Several of the pending claims have been amended in order to more fully and/or definitely claim Applicants' invention. New claims have been added in order to more fully protect Applicants' invention. A Terminal Disclaimer is attached hereto to address the Examiner's concern of obviousness-type double patenting. No new matter has been added.

OFFICE ACTION

In the Office Action dated May 19, 2000, claims 151-156, 159-160, 161-167 and 171-175 were rejected under the judicially created doctrine of obviousness-type double patenting over claims 2-5, 13, 20-23, and 29 of U.S. Patent 6,034,918. Claims 157-158, and 168 were rejected under the judicially created doctrine of obviousness-type double patenting over claims 16-17 and 33 of U.S. Patent 6,034,918.

NONSTATUTORY DOUBLE PATENTING

To address the concern regarding double patenting in light of U.S. Patent 6,034,918 and in an effort to expedite the prosecution of this application, Applicants submit herewith a Terminal Disclaimer executed by the attorney of record in this application. The Terminal Disclaimer is submitted to obviate the double patenting rejection over U.S. Patent 6,034,918. Applicants believe that the Terminal Disclaimer complies fully with the relevant parts of 37 CFR S 1.321.

NEWLY SUBMITTED CLAIMS

The new claims submitted in this Amendment have been added to more definitely and fully protect Applicants' invention. No new matter has been added.

INFORMATION DISCLOSURE STATEMENT

In compliance with the duty of disclosure set forth in 37 CFR §1.56, Applicants submit concurrently herewith an Information Disclosure Statement, a modified Form PTO-1449, and a copy of the documents cited therein. A _copy_ of that Information Disclosure Statement and modified Form PTO-1449 are attached hereto.

Several of the documents listed in the modified Form PTO-1449 have been recently identified by a respondent in a pending ITC investigation, namely in re <u>U.S. International Trade Commission Investigation No. 337-TA-431, Rambus Inc. vs Hitachi Ltd., et al.</u>, as prior art against the inventions claimed in the parent patent (i.e., U.S. Patent 6,034,918) of the instant application. An explicit reference to these documents is made in paragraph 17 on page 28, as well as in Exhibit A, of the RESPONSE OF HITACHI LTD. TO THE COMPLAINT AND NOTICE OF INVESTIGATION (hereinafter the "RESPONSE"). A copy of the RESPONSE is also included with the Information Disclosure Statement submitted concurrently herewith.
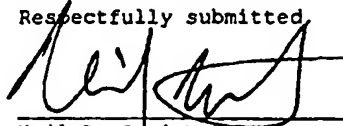
It is respectfully requested that the Examiner make his consideration of the documents cited in the Form PTO-1449 formally of record with the next Action. In accordance with 37 C.F.R. §1.97(c), the fee set forth in 37 C.F.R. §1.17(p) accompanies that Statement.

Page 5

CONCLUSION

Applicants request entry of the foregoing amendment. Applicants submit that all of the claims present patentable subject matter which definitely set forth the novel and unobvious features of Applicants' invention. Accordingly, Applicants respectfully request allowance of all of the claims.

It is noted that should a telephone interview expedite the prosecution in any way, the Examiner is invited to contact Neil Steinberg at 650-944-7772.

Respectfully submitted,

Date: June 2, 2000

Neil A. Steinberg
Reg. No. 34,735
650-944-7772

Page 6

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
(Case No. P043D2C3C)

In the Application of: **RECEIVED**   )
)

FARMWALD et al.   JUN **15** 2000   )

Serial No: 09/492,982   TECHNOLOGY CENTER 2800   )
                          SPECIAL PROGRAM CENTER

Filed: JANUARY 27, 2000   )

Title: METHOD OF OPERATING A MEMORY   )
       DEVICE HAVING A VARIABLE DATA   )
       INPUT LENGTH   )

Group
Art Unit: 2818

Before
Examiner: T. Nguyen

Assistant Commissioner for Patents
Washington, DC 20231

<u>TERMINAL DISCLAIMER TO OBVIATE A
DOUBLE PATENTING REJECTION OVER A PRIOR PATENT</u>

Dear Sir:

The owner, Rambus Inc., of the entire right, title and interest
in the instant application, hereby disclaims, except as provided below,
the terminal part of the statutory term of any patent granted on the
instant application, which would extend beyond the expiration date of
the full statutory term defined in 35 U.S.C. 154 to 156 and 173, as
presently shortened by any terminal disclaimer, of U.S. Patent
6,034,918. The owner hereby agrees that any patent so granted on the
instant application shall be enforceable only for and during such
period that it and the prior patent are commonly owned. This agreement
runs with any patent granted on the instant application and is binding
upon the grantee, its successors or assigns.
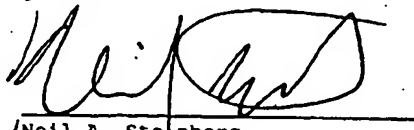
In making the above disclaimer, the owner does not disclaim the
terminal part of any patent granted on the instant application that

06/07/2000 SHUNG 00000023 500998 09492982
02 FC:148   110.00 CH

Page 1

would extend to the expiration date of the full statutory term as defined by 35 U.S.C. 154 to 156 and 173 of the prior patent, as presently shortened by any terminal disclaimer, in the event that it later expires for failure to pay a maintenance fee, is held unenforceable, is found invalid by a court of competent jurisdiction, is statutorily disclaimed in whole or terminally disclaimed under 37 C.F.R. 1.321, has all claims canceled by a reexamination certificate, is reissued, or is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under § 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

The undersigned is the attorney of record.

Date: June 2, 2000

/Neil A. Steinberg
Reg. No. 34,735
650-944-7772

TERMINAL DISCLAIMER
APPROVED

JUN 1 5 2000

TECHNOLOGY CENTER 2800
SPECIAL PROGRAM CENTER

Page 2

G A4 28188

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
(P043D2C3C)

In re Application of:)
)
FARMWALD ET AL.   )
)   Art Unit: 2818
Serial No: 09/492,982   )
)
Filed: JANUARY 27, 2000   )   Examiner: T. Nguyen
)
Title: METHOD OF OPERATING A MEMORY DEVICE   )
            HAVING A VARIABLE DATA INPUT LENGTH   )   RECEIVED

                                                         JUN 0 6 2000

Commissioner of Patents and Trademarks   TECHNOLOGY CENTER 2800
Washington, D.C. 20231

Dear Sir:
        With respect to the above-identified application, transmitted herewith is an AMENDMENT,
STATUTORY TERMINAL DISCLAIMER and INFORMATION DISCLOSURE STATEMENT.

The fee has been calculated as shown below:

CLAIMS AS AMENDED						
	Claims Remaining After Amendment	Highest Number Previously Paid For	Extra	Rate		Amount
				Large Entity	Small Entity	
Number of Claims in Excess of 20	27	25	2	$ 18.00	$ 9.00	$36.00
Independent Claims in Excess of 3	3	3	0	$ 78.00	$ 39.00	$0.00
First Presentation of Multiple Dependent Claims				250.00	125.00	-0-
Submission of a Statutory Terminal Disclaimer -- 37 CFR 1.20(d)						$110.00
Submission of Information Disclosure Statement under 37 CFR §1.97(c)						$240.00
					TOTAL FEE DUE:	$386.00

[XX] Please charge my Deposit Account No. 50-0998 in the amount of $386.00 to cover the above fees. A duplicate
     copy of this sheet is enclosed.

[XX] The Commissioner is hereby authorized to charge any fees which may be required, or credit any
     overpayment to Deposit Account No. 50-0998. A duplicate copy of this sheet is enclosed.

                                                     Respectfully submitted,

Date: June 2, 2000   By: _____
                                                         Neil A. Steinberg
                                                         Registration No. 34,735
                                                         650-944-7772

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
(Case No. P043D2C3C)

In the Application of:	)
	)
FARMWALD, ET AL.	)
	)
Serial No.: 09/492,982	)
	)
Filed: JANUARY 27, 2000	)
	)
Title: METHOD OF OPERATING A MEMORY	)
DEVICE HAVING A VARIABLE DATA	)
INPUT LENGTH	)

Assistant Commissioner for Patents
Washington, DC 20231

Certificate of Mailing Under 37 CFR 1.8

I hereby certify that the attached 1) Transmittal Letter (1 page and 1 copy

thereof), 2) Amendment (6 pages and 4 page attachment), 3) Terminal Disclaimer to

Obviate a Double Patenting Rejection Over a Prior Patent (2 pages), 4) Information

Disclosure Statement (4 pages and documents cited in IDS) is/are being deposited with

the United States Postal Service with sufficient postage as first-class U.S. mail in an

envelope addressed to:

Assistant Commissioner for Patents
Washington, D.C. 20231

on June 2, 2000.

Michiko Sites
(Signature)

Michiko Sites

(Print Name of Person Signing Certificate)

863 FH PG 0244

Office Action Summary

Application No.	Applicant(s)
09/492,982	FRIEDWALD et al.
Examiner	Group Art Unit
TAN T. NGUYEN	2818

—The MAILING DATE of this communication appears on the cover sheet beneath the correspondence address—

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE __-3-__ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

☑ Responsive to communication(s) filed on __06/05/00__

☐ This action is FINAL.

☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

☑ Claim(s) __151 - 177__ is/are pending in the application.

    Of the above claim(s) __1 - 150__ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☑ Claim(s) __151, 152, 153, 156, 159-163, 166, 167, 171, 172, 174, 175__ is/are rejected.

☑ Claim(s) __154-155, 157-158, 164-165, 168-170, 173, 176-177__ is/are objected to.

☐ Claim(s) _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119 (a)-(d)

☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

    ☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

    ☐ received.

    ☐ received in Application No. (Series Code/Serial Number) _____

    ☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

    *Certified copies not received: _____

Attachment(s)

☑ Information Disclosure Statement(s), PTO-1449, Paper No(s). __5__

☐ Notice of Reference(s) Cited, PTO-892

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Interview Summary, PTO-413

☐ Notice of Informal Patent Application, PTO-152

☐ Other _____

Office Action Summary

1.   The following action is in response to the amendment filed by Applicants on June 5, 2000.

2.   The Information Disclosure Statement submitted by Applicants on June 5, 2000 has been

received and fully considered.

3.   The Terminal Disclaimer filed by Applicants on June 5, 2000 has been received.

4.   New claims 176-177 have been entered.

5.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or
> on sale in this country, more than one year prior to the date of application for patent in the United States.

6.   Claims 151-153, 156, 159-163, 166-167, 171-172 and 174-175 are rejected under 35

U.S.C. 102(b) as being anticipated by Laid-open Patent Application No. 60-55459 (hereinafter JP

'459).

        JP '459 disclosed in figure 4 a block data transfer method and storage control method in

which the number of words to be transferred is provided to the memory control device [2] via bus

[7] (page 5, lines 11-13) and then in response to a write request (page 3, line 22), the data block

is written to the destination memory area.

        It is inherent that the data is in binary form, and the memory device disclosed by JP '459 is

operated in synchronous with clock signal.
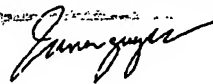
7.   Claims 154-155, 157-158, 164-165, 168-170, 173 and 176-177 are objected to as being

dependent upon a rejected base claim, but would be allowable if rewritten in independent form

including all of the limitations of the base claim and any intervening claims.

8.   Any inquiry concerning this communication or earlier communications from the examiner

should be directed to Tan T. Nguyen whose telephone number is (703) 308-1298. The examiner

can normally be reached on Monday to Friday from 04:00 AM to 04:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor,

Mr. David C. Nelms, can be reached on (703) 308-4910. The fax phone number for the

organization where this application or proceeding is assigned is (703) 308-7724.

Any inquiry of a general nature or relating to the status of this application or proceeding

should be directed to the receptionist whose telephone number is (703) 308-0956.

Tan T. Nguyen
Primary Examiner
Art Unit 2818
July 31, 2000

T.N
07/31/00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
(Case No. P043D2C3C)

In the Application of:)
)
FARMWALD et al.)
)
Serial No: 09/492,982)
)
Filed: JANUARY 27, 2000)
)
Title: METHOD OF OPERATING A MEMORY)
        DEVICE HAVING A VARIABLE DATA)
        INPUT LENGTH)

Group
Art Unit: 2818

Before
Examiner: T. Nguyen

Assistant Commissioner for Patents
Washington, DC 20231

AMENDMENT

Dear Sir:

In response to the Office Action dated August 1, 2000, kindly amend the application as follows:

IN THE CLAIMS:

Kindly amend the following claims:

In claim 158, line 1, replace "156" with --157--.

In claim 159, line 2, after the first occurrence of "the", insert --first--.

In claim 161, line 3, delete the second occurrence of "of" and substitute --in--.

In claim 163, line 5, delete "bus".

In claim 171, line 6, delete "from a bus".

REMARKS

This Amendment seeks to place this application in condition for allowance. All of the Examiner's rejections have been addressed. Several of the pending claims have been amended. No new matter has been added.

OFFICE ACTION

In the Office Action mailed August 1, 2000, claims 151-153, 156, 159-163, 166-167, 171-172 and 174-175 were rejected as being anticipated by Japanese Laid-Open Patent Application No. 60-55459 (hereinafter "the '459 application"). The remaining claims, namely claims 154, 155, 157, 158, 164, 165, 168-170, 173, 176 and 177, were objected to as being dependent upon the rejected claims.

Rejection - 35 U.S.C. § 102:

Applicants respectfully disagree with the Examiner's position that the rejected claims are anticipated by the '459 application.[1] The Examiner stated that the '459 application discloses in figure 4, a block data transfer method and storage control method in which the number of words to be transferred is provided to memory control device

---

[1] The rejection here is based on prior art which similar in many respects to the prior art, namely Jackson, U.S. Patent 4,315,308, which formed the basis of the 35 U.S.C. §102 rejection made in the parent application (App. Ser. No. 09/252,997, now, U.S. Patent 6,034,918).

Page 2

via bus [7](page 5, lines 11-13) and then in response to a write request (page 3, line 22), the data block is written to the destination memory area. While this may be true, memory 1 disclosed in the '459 application -- unlike the claimed invention -- is _not_ provided nor does it receive information indicating the "number of words to transfer"[2] as required by the claims of the instant application. For example, claim 161 (as amended) recites in pertinent part:

> A method of operation in a synchronous memory device, ...
> the method of operation in the memory device comprises:
> receiving first block size information from a controller, wherein the first block size information defines a first amount of data to be input by the memory device in response to a write request

The memory in the '459 application does not receive block size information. Rather, the memory of the '459 application responds to the sequentially applied address and control signals from the memory control device 2 in order to store the appropriate number of words in memory 1.

It is the memory control device 2 of the '459 application which receives, decodes and stores the information indicating the number of words to be stored in memory 1. In this regard, the memory control device 2 stores the number of words in a counter, and, based thereon, generates and sequentially applies the appropriate address and control

---

[2]For the purposes of this discussion, the phrase "number of words to transfer" may be assumed to correspond to "block size information".

Page 3

signals necessary to write the words to memory 1. The information indicating the number of words to transfer is **not** provided to the memory (and as such, the memory does not receive such information) in the '459 application.

The '459 application

The '459 application discloses a system including memory 1, memory control device 2, cache memory 3, a main processing device 4, and an input/output processing device 5. (See Figure 2). The memory 1 is connected to memory control device 2 via memory bus 6. Memory control device 2 and input/output processing device 5 are both connected to bus 7 (See, the '459 application, page 3 lines 11-16, and Figure 2).

Communication between memory 1 and devices connected to bus 7 is executed via memory control device 2. In this regard, the '459 application states that "control of reading or writing from memory 1 is performed by memory control device 2 via memory bus 6." (page 3, line 13-14). The memory control device 2 controls memory 1 via a memory interface which includes memory address signal 242, memory data (bus) 243 and memory response signal 240. (See, the '459 application, page 6, lines 17-21). Address signal 242 and data 243 are employed to transfer address and data, respectively, between memory control device 2 and memory 1. (See, the '459 application, page 6 lines 18-21 and Figure 6).

In operation, a "number of words to transfer," together with origin and destination addresses, are provided to memory control device

Page 4

863 FH PG 0251

863 FH PG 0251

2. (See, e.g., the '459 application, page 4, lines 36-39). Memory control device 2 increments or decrements source and destination address counters while maintaining a count of the number of remaining words to be transferred to memory 1. In this regard, the '459 application, on page 5, lines 21-24 states:

> The counter for the remaining number of words to transfer, which is set with number of words to transfer, is decremented each time data is transferred and stored, and when that count value reaches zero, transfer ... ends.

The memory control device 2 of the '459 application, at all times, maintains the information regarding the number of words to transfer, generates the appropriate control and address signals, and applies the control and address signals which are necessary to transfer the requested number of words to memory 1. (See, the '459 application, page 7, lines 26-39, and Figure 9). The memory control device 2 receives, decodes and stores, in a counter 203, information indicating the number of words to transfer to memory 1 and, based thereon generates address and control signals and sequentially applies those addresses and control signals in order to transfer the indicated number of words from memory 1. The memory control device 2 does not provide information indicating the number of words to transfer to memory 1.

Page 5

Although the '459 application does not describe memory 1 in great detail,[3] memory 1 is most likely a standard off-the-shelf memory device or memory module incorporating the same, for example, memory devices like those described in the Kung et al., U.S. Pat. 4,449,207, and Voss, U.S. Pat. 4,646,270. The memory 1 described in the '459 application does not appear to input or output data synchronously with respect to a clock signal. Instead, control signals such as function signal 241 and memory response signal 240, generated by memory control device 2, are employed to signal the transfer of data between memory 1 and memory control device 2. (See, the '459 application, Figure 9, and page 7, lines 26-34). The writing of data to memory 1 from memory control device 2 is described on page 7, lines 31-34 as follows:

> ...after response 240 is acquired, if memory function signal 241 is made the write mode [ ] the contents of transfer destination address counter 203 are output as memory address signal 242, memory data 243 is transferred to and stored at the transfer destination memory area."

The '459 application Does Not Anticipate Claims 151 and 152

Claim 151 is directed to a method of controlling a memory device and requires, among other things, providing first block size information to the memory. The first block size information defines a first amount of data to be input by the memory device in response to a write request.

---

[3] The '459 application suggests the use of "The latest dynamic RAMs" featuring "Nibble Mode Support" as in "*Nikkei Electronics, April 1983.*" (see page 8, lines 38-39).

As mentioned above, information indicating the number of words to be transferred by the memory control device 2 is not provided to memory 1. Instead, memory control device 2 of the '459 application receives, decodes and stores that information in a counter, and, based thereon, sequentially generates the address and control signals necessary to write the words to the memory device. In this regard, the system described in the '459 application is similar to the system described in Jackson, U.S. Pat. 4,315,308. The claims of the parent (i.e., App. Ser. No. 09/252,997, now, U.S. Pat. 6,034,918) of the instant application were initially rejected as being anticipated by Jackson but ultimately found patentable over Jackson.

Importantly, memory 1 of the '459 application does not receive information indicating the number of words to be transferred. The memory 1 simply responds to the sequentially applied address and control signals provided by memory control device 2.

Thus, for at least these reasons, the '459 application does not anticipate claim 151 or the claims which depend therefrom.[4]

---

[4] It should be noted that claim 152 requires that the memory device input the data synchronously with respect to an external clock signal. The memory disclosed in the '459 application does not input data in this manner.

Page 7

The '459 application Does Not Anticipate Claims 161 and 162

Claim 161 is directed to a method of operation in a memory device, and, like claim 151, requires that the memory device _receive_ first block size information.

For reasons similar to those mentioned above, the memory disclosed in the '459 application does not receive the information indicating the number of words to be transferred. The memory of the '459 application simply responds to the sequentially applied address and control signals from the memory control device 2. The memory control device 2 receives, decodes and stores information that indicates the number of words to be transferred to memory 1 in a counter, and, based thereon, generates and sequentially applies the appropriate address and control signals necessary to write the appropriate number of words to memory 1. The information indicating the number of words to be transferred is _not_ provided to memory 1.

Thus, for _at least_ these reasons, the '459 application does not anticipate claim 161 or the claims which depend therefrom.

The '459 application Does Not Anticipate Claim 171

Claim 171 is directed to a method of operation of an integrated circuit, wherein the integrated circuit includes a memory array. Claim 171 requires, among other things, that the integrated circuit ~~receive~~ block size information. The memory device disclosed in the '459 application does _not_ receive the information indicating the number of

Page 8
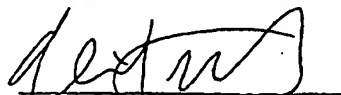
words to transfer. Thus, for <u>at least</u> this reason, the '459 application does not anticipate claim 171 or its dependent claims.

<u>CONCLUSION</u>

Applicants request entry of the foregoing Amendment. Applicants submit that all of the claims present patentable subject matter. Accordingly, allowance of all of the claims is respectfully requested.

It is noted that should a telephone interview expedite the prosecution in any way, the Examiner is invited to contact Neil Steinberg at 650-944-7772.

Respectfully submitted,

Date: October 31, 2000

Neil A. Steinberg
Reg. No. 34,735
650-944-7772

Page 9

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
(P043D2C3C)

In re Application of:

FARMWALD ET AL

Serial No: 09/492,982

Filed: JANUARY 27, 2000

Title: METHOD OF OPERATING A MEMORY DEVICE
           HAVING A VARIABLE DATA INPUT LENGTH

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)
)
)   Art Unit: 2818
)
)
)   Examiner: T. Nguyen
)
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Commissioner of Patents and Trademarks
Washington, D.C. 20231

BOX: NON-FEE AMENDMENT

Dear Sir:

With respect to the above-identified application, transmitted herewith is an AMENDMENT (9 pages).

[ ]   Please charge my Deposit Account No. 50-0998 in the amount of $___ to cover the above fees. A duplicate
      copy of this sheet is enclosed.

[XX] The Commissioner is hereby authorized to charge any fees which may be required, or credit any
      overpayment to Deposit Account No. 50-0998. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

Date: October 31, 2000

By:

Neil A. Steinberg
Registration No. 34,735
650-944-7772

20''

Ms. Michiko Sites
RAMBUS INC.
2465 Latham Street
Mountain View, California   94040

Serial/Patent No.: 09/492,982   Filing/Issue Date: January 27, 2000
Title: Method of Operating a Memory Device Having a Variable Data Input Length
Atty. Docket No.: RA043D2C3C   Date Mailed: October 31, 2000

The following has been received in the U.S. Patent & Trademark Office on the date stamped hereon:

☒ Amendment/Response (9 pgs.)   ☐ Petition for Extension of Time (month(s))
☐ Preliminary Amendment (pgs.)   ☐ Information Disclosure Statement & PTO 1449
☐ Application - Utility (pgs., with cover and abstract)   ☐ Issue Fee Transmittal
☐ Application - Rule 1.53(b) Continuation (pgs.)   ☐ Submission of Formal Drawings
☐ Application - Rule 1.53(b) Divisional (pgs.)   ☐ Notice of Appeal
☐ Application - Rule 1.53(b) CIP (pgs.)   ☐ Appeal Brief (pgs. in triplicate)
☐ Application - Rule 1.53(d) CPA (pgs.)   ☐ Reply Brief
☐ Application - PCT (pgs.)   ☐ Response to Notice of Missing Parts
☐ Application - Provisional (pgs.)   ☒ Transmittal Letter (in duplicate)
☐ Drawings (14 sheets)   ☐ Fee Transmittal (in duplicate)
☐ Declaration & POA (pgs.)   ☒ Itemized Postcard
☐ Assignment & Cover Sheet   ☒ Certificate of Mailing
☐ Power of Attorney   ☐ Express Mail No.
☐ Other Cross Reference Under 37 C.F.R. Sec.1.78

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
(Case No. P043D2C3C)

In the Application of:

    FARMWALD et al.

Serial No: 09/492,982

Filed: JANUARY 27, 2000

Title: METHOD OF OPERATING A MEMORY
DEVICE HAVING A VARIABLE DATA
INPUT LENGTH

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Group
Art Unit:

Before
Examiner: T. Nguyen

Assistant Commissioner for Patents
Washington, DC 20231

AMENDMENT

Dear Sir:

In response to the telephone interview of November 21 2000, kindly amend the application as follows:

<u>IN THE CLAIMS</u>:

Kindly **delete** claim 175 (without prejudice).

Kindly **amend** the following claims:

Page 1

151. (Amended) A method of controlling a memory device by a memory controller, wherein the memory device includes a plurality of memory cells, the method of controlling the memory device comprises:

    providing first block size information to the memory device, wherein the first block size information is provided by the memory controller and defines a first amount of data to be input by the memory device in response to a write request; and

    issuing a first write request to the memory device, wherein in response to the first write request the memory device inputs the first amount of data corresponding to the first block size information.

171. (Twice Amended) A method of operation of an integrated circuit, wherein the integrated circuit includes a memory array having a plurality of memory cells, the method of operation comprises:

    receiving block size information from a controller, wherein the block size information defines a first amount of data to be input in response to a write request;

    receiving a first write request; and

    inputting the first amount of data corresponding to the block size information in response to the first write request.

REMARKS

This Amendment seeks to place this application in condition for allowance. In the telephone interview on November 21, 2000, the Examiner expressed a concern that claim 151 could be interpreted in such a way as to read on Japanese Laid-Open Patent Application No. 60-55459 (hereinafter "the '459 application"). While the Examiner recognized that memory 1 of the '459 application does not receive block size information, the Examiner expressed concern that the memory control device 2 together with memory 1 could be considered as the "memory device" of claim 151. While Applicants do not agree with this point of view, nevertheless Applicants have amended claim 151 to more particularly point out and distinctly claim the invention to recite a method of controlling a memory device by a memory controller. Amended claim 151 also requires, among other things, that the first block size information is provided by the memory controller. Thus, both the memory controller and the memory device are expressly set forth in claim 151.

Applicants submit that all of the claims present patentable subject matter which definitely set forth the novel and unobvious features of Applicants' invention. Accordingly, Applicants respectfully request allowance of all of the claims.

It is noted that should a telephone interview expedite the prosecution in any way, the Examiner is invited to contact Neil Steinberg at 650-944-7772.

Respectfully submitted,

Date: November 22, 2000

Neil A. Steinberg
Reg. No. 34,735
650-944-7772

Page 3

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
(Case No. P043D2C3C)

In the Application of:)
)
    FARMWALD et al.   )
)   Group
Serial No: 09/492,982   )   Art Unit: 2818
)
Filed: JANUARY 27, 2000   )   Before
)   Examiner: T. Nguyen
Title: METHOD OF OPERATING A MEMORY   )
       DEVICE HAVING A VARIABLE DATA   )
       INPUT LENGTH   )

Assistant Commissioner for Patents
Washington, DC 20231

INFORMATION DISCLOSURE STATEMENT

Dear Sir:

    In compliance with the duty of disclosure set forth in 37 C.F.R.
§1.56, submitted herewith is a modified Form PTO-1449, including a copy
of all of the documents listed therein. In accordance with 37 C.F.R.
§1.97(c), authorization to charge Applicant's deposit account for the
fee set forth in 37 C.F.R. §1.17(p) accompanies this statement.

    All of the documents listed in the PTO-1449 have been recently
identified by a Plaintiff in a pending U.S. District Court For The
Northern District of California case, namely in Hyundai et al. v.
Rambus Inc., as prior art against the inventions claimed in the parent
patent (i.e., U.S. Patent 6,034,918) of the instant application. An
explicit reference to these documents is made on pages 24-25 of the
INITIAL DISCLOSURE OF PRIOR ART UNDER LOCAL RULES 16-7 AND 16-8.

Page -1-

(hereinafter the "INITIAL DISCLOSURE"). A copy of the INITIAL DISCLOSURE is also submitted herewith.

It is respectfully requested that the Examiner make his consideration of these references formally of record with the next Action.

Respectfully submitted,

Date: November 17, 2000

Neil A. Steinberg
Reg. No. 34,735
650-944-7772

PTO-1449 (Modified)	ATTY. DOCKET NO. P043D2C3C	SERIAL NUMBER 09/492,982
U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	APPLICANT(S) FARMWALD ET AL.	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	FILING DATE JANUARY 27, 2000	GROUP ART UNIT 2818

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
TNT	3,691,534	09/12/72	Veradi, et. al	365	78	
	3,771,145	11/06/73	Wiener	365	240	
	4,231,104	10/28/80	St.Clair	713	500	
	4,466,127	08/14/84	Ohgishi, et. al	455	182.1	
	4,536,795	08/20/85	Hirota, et. al	348	714	
	4,616,268	10/07/86	Shida, et. al	358	451	
	4,629,909	12/16/86	Cameron	327	211	
	4,631,659	12/23/86	Hayne, et. al	711	167	
TNT	4,648,102	03/03/87	Riso, et. al	375	356	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO
TNT	EP 0424774	05/02/91	EPO	—	—	
TNT	EP 0449052	03/29/90	EPO	—	—	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

TNT	Takasugi, A. et al., "A Data-Transfer Architecture for Fast Multi-Bit Serial Acess Mode DRAM," 11th European Solid State Circuits Conference, Toulouse, France pp.161-165 (Sep. 1985)
TNT	Amitai, Z., "Burst Mode Memories Improve Cache Design," WESCON/90 Conference Record, pp.79-82 (Nov. 1990)
TNT	Ikeda, Hiroaki et al., "100 MHz Serial Acess Architecture for 4Md Field Memory," Symposium of VLSI Circuits, Digest of Technical Papers, pp. 11-12 (Jun. 1990)
TNT	Schmitt-Landsiedel, Doris, "Pipeline Architecture for Fast CMOS Buffer RAMs," IEEE Journal of Solid-State Circuits, Vol. 25, No. 3, pp. 741-747 (Jun. 1990)

EXAMINER TON T. NGUYEN	DATE CONSIDERED 11/27/00

EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant.

PTO-1449 (Modified) ⁹	ATTY. DOCKET NO. P043D2C3C	SERIAL NUMBER 09/492,982
U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	APPLICANT(S) FARMWALD ET AL	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	FILING DATE JANUARY 27, 2000	GROUP ART UNIT 2818

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
TNT	4,663,735	05/05/87	Novak, et. al	345	515	
	4,672,470	06/09/87	Morimoto, et. al	386	16	
	4,719,505	01/12/88	Katznelson	348	502	
	4,825,287	04/25/89	Baji, et. al	348	720	
	4,845,677	07/04/89	Chappell, et. al	365	189.02	
	4,873,671	10/10/89	Kowshik, et. al	365	189.12	
	4,876,670	10/24/89	Nakabayashi, et. al	365	194	
TNT	4,901,036	02/13/90	Herold, et. al	331	25	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO
TNT	EP 0218523	05/30/89	EPO			
TNT	EP 0282735	09/21/88	EPO			

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

TNT	K. Ohta, "A 1-Mbit DRAM with 33-MHz Serial I/O Ports", IEEE Journal of Solid State Circuits, vol. 21 No. 5, pp. 649-654 (Oct. 1986)
TNT	Horowitz et al., "MIPS-X: A 20-MIPS Peak 32-Bit Microprocessor with ON-Chip Cache", IEEE J. Solid State Circuits, vol. SC-22, No. 5, pp. 790-798 (Oct. 1987)
TNT	Robert J. Lodi et al., "Chip and System Characteristics of a 2048-Bit MNOS-BORAM LSI Circuit," 1976 IEEE International Solid-State Circuits Conference (Feb. 18, 1976)

EXAMINER Tan T. Nguyen	DATE CONSIDERED 4/27/00

EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant.

PTO-1449 (Modified)	ATTY. DOCKET NO. P043D2C3C	SERIAL NUMBER 09/492,982
U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	APPLICANT(S) FARMWALD ET AL	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	FILING DATE JANUARY 27, 2000	GROUP ART UNIT 2818

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
TNT	4,979,145	12/18/90	Remington, et. al	711	106	
	5,009,481	04/23/91	Kinoshita, et. al	385	33	
	5,016,226	05/14/91	Hiwada, et. al	365	233	
	5,036,495	07/30/91	Busch, et. al	365	233	
	5,111,486	05/05/92	Oliboni, et. al	375	120	
	5,123,100	06/16/92	Hisada, et. al	713	401	
	5,142,376	08/25/92	Ogura	386	29	
TNT	5,276,846	01/04/94	Aichelmann Jr., et. al	711	165	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

TNT	Whiteside, Frank, "A Dual-Port 65ns 64Kx4 DRAM with a 50MHz Serial Output," IEEE International Solid-State Circuits Conference Digest (Feb. 1986)

EXAMINER Tan T. Nguyen	DATE CONSIDERED 4/27/00

EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant.

PTO-1449 (Modified) |	ATTY. DOCKET NO. P043D2C3C	SERIAL NUMBER 09/492,982
U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	APPLICANT(S) FARMWALD ET AL.	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	FILING DATE JANUARY 27, 2000	GROUP ART UNIT 2818

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
TNi	5,301, 278	04/05/95	Bowater, et al	711	5	
	5,361,277	11/01/94	Grover	375	38	
TNi	5,684,753	11/04/97	Hashimoto, et al	365	233	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO
TNi	WO 89/12936	12/28/89	PCT			
	JP 62-51509	03/06/87	Japan			YES

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

TNi	Pinkham, Raymond, "A High Speed Dual Port Memory with Simultaneous Serial and Random Mode Access for Video Applications," IEEE Journal of Solid-State Circuits, Vol. SC-19, No. 6, pp. 999-1007 (Dec. 1984)
TNi	Ishimoto, S. et al., "A 256K Dual Port Memory," ISSCC Digest of Technical Papers, p. 38-39 (Feb. 1985)
TNi	Iqbal, Mohammad Shakaib, "Internally Timed RAMs Build Fast Writable Control Stores," Electronic Design, pp. 93-96 (August 25, 1988)
TNi	Schnaitter, William M. et al., "A 0.5-GHz CMOS Digital RF Memory Chip," IEEE Journal of Solid-State Circuits, vol. SC-21, no. 5, pp. 720-726 (Oct. 1986)
TNi	Bursky, Dave, "Advanced Self-Timed SRAM Pares Access Time to 5 ns," Electronic Design, pp. 145-147 (Feb. 22, 1990)
TNi	Tomoji Takada et al., "A Video Codec LSI for High-Definition TV Systems with One-Transistor DRAM Line Memories," IEEE Journal of Solid-State Circuits, Vol. 24, No. 6, pp. 1656-1659 (Dec. 1989)

EXAMINER Tan T. Nguyen	DATE CONSIDERED 4/27/00

EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant.

PTO-1449 (Modified)		ATTY. DOCKET NO. P043D2C3C	SERIAL NUMBER 09/492,982
U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		APPLICANT(S) FARMWALD ET AL.	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT		FILING DATE JANUARY 27, 2000	GROUP ART UNIT 2818

U.S. PATENT DOCUMENTS

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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

TNT	Robert J. Lodi et al., "MNOS-BORAM Memory Characteristics," IEEE Journal of Solid-State Circuits, vol. SC-11, No. 5, pp. 622-631 (Oct. 1976)
TNT	Gregory Uvieghara et al., "An On-Chip Smart Memory for a Data-Flow CPU," IEEE Journal of Solid-State Circuits, vol. 25, No. 1, pp. 84-89 (Feb. 1990)
TNT	Ray Pinkham et al., "A 128Kx8 70-MHz Multiport Video RAM with Auto Register Reload and 8x4 WRITE Feature," IEEE Journal of Solid State Circuits, vol. 23, no. 3, pp. 1133-1139 (Oct. 1988)
TNT	Hans-Jurgen Mattausch et al., "A Memory-Based High-Speed Digital Delay Line with a Large Adjustable Length," IEEE Journal of Solid-State Circuits, vol. 23, no. 1, pp. 105-110 (Feb. 1988)
TNT	Kanopoulos, Nick and Jill H. Hallenbeck, "A First-In, First-Out Memory for Signal Processing Applications," IEEE Transactions on Circuits and Systems, Vol. CAS-33, No. 5, pp. 556-558 (May 1986)

EXAMINER TAN T. NGUYEN	DATE CONSIDERED 4/27/00

EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
(P0043D2C3C)

In re Application of:	)
	)
FARMWALD ET AL.	)
	) Art Unit: 2818
Serial No: 09/492,982	)
	)
Filed: JANUARY 27, 2000	) Examiner: T. Nguyen
	)
Title: METHOD OF OPERATING A MEMORY DEVICE	)
HAVING A VARIABLE DATA INPUT LENGTH	)

RECEIVED
NOV 27 2000
TECHNOLOGY CENTER 2800

Commissioner of Patents and Trademarks
Washington, D.C. 20231

Dear Sir:

With respect to the above-identified application, transmitted herewith is an INFORMATION DISCLOSURE STATEMENT and an AMENDMENT.

Fees:	
For submission of Information Disclosure Statement under 37 CFR §1.97(c), the fee set forth in 37 CFR §1.17(p)	$240.00
TOTAL FEE DUE:	$240.00

[·] A check payable to the Commissioner of Patents and Trademarks, in the amount of $_____ is enclosed as payment of the Total Fee Due.

[XX] Please charge my Deposit Account No. 50-0998 in the amount of $240.00 to cover the above fees. A duplicate copy of this sheet is enclosed.

[XX] The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 50-0998. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

Date: November 22, 2000

By: _____
Neil A. Steinberg
Registration No. 34,735
650-944-7772

Ms. Michiko Sites
RAMBUS INC.
2465 Latham Street
Mountain View, California 94040

Serial/Patent No.: 09/492,982
Title: Method of Operating a Memory Device Having a Variable Data Input Length
Atty. Docket No.: RA013D2C3C

Filing/Issue Date: January 27, 2000
Date Mailed: November 22, 2000

The following has been received in the U.S. Patent & Trademark Office on the date stamped hereon:

☒ Amendment/Response (3 pgs.)
☐ Preliminary Amendment (pgs.)
☐ Application - Utility (pgs., with cover and abstract)
☐ Application - Rule 1.53(b) Continuation (pgs.)
☐ Application - Rule 1.53(b) Divisional (pgs.)
☐ Application - Rule 1.53(b) CIP (pgs.)
☐ Application - Rule 1.53(d) CPA (pgs.)
☐ Application - PCT (pgs.)
☐ Application - Provisional (pgs.)
☐ Drawings (14 sheets)
☐ Declaration & POA (pgs.)
☐ Assignment & Cover Sheet
☐ Power of Attorney
☐ Other Cross Reference Under 37 C.F.R. Sec.1.78

☐ Petition for Extension of Time (month(s))
☒ Information Disclosure Statement & PTO 1449
☐ Issue Fee Transmittal
☐ Submission of Formal Drawings
☐ Notice of Appeal
☐ Appeal Brief (pgs. in triplicate)
☐ Reply Brief
☐ Response to Notice of Missing Parts
☒ Transmittal Letter (in duplicate)
☐ Fee Transmittal (in duplicate)
☒ Itemized Postcard
☐ Certificate of Mailing
☐ Express Mail No.

09/492982

APPLICATION NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.

09/492,982   01/27/00   FARMWALD

MMC1/1128

M   P043D2C3C

EXAMINER

Neil A Steinberg Esq
Rambus Inc
2465 Latham Street
Mountain View CA 94040

ART UNIT NGUYEN PAPER NUMBER

/2

2818
DATE MAILED:

11/28/00

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

NOTICE OF ALLOWABILITY

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance and Issue Fee Due or other appropriate communication will be mailed in due course.

☑ This communication is responsive to _the Amendment filed on 11/27/00_

☑ The allowed claim(s) is/are _151 - 174 and 176 - 177_

☐ The drawings filed on _____ are acceptable.

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

A SHORTENED STATUTORY PERIOD FOR REPLY to comply with the requirements noted below is set to EXPIRE THREE MONTHS FROM THE "DATE MAILED" of this Office action. Failure to timely comply will result in ABANDONMENT of this application. Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

☐ Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL APPLICATION, PTO-152, which discloses that the oath or declaration is deficient. A SUBSTITUTE OATH OR DECLARATION IS REQUIRED.

☑ Applicant MUST submit NEW FORMAL DRAWINGS

☐ because the originally filed drawings were declared by applicant to be informal.

☑ including changes required by the Notice of Draftperson's Patent Drawing Review, PTO-948, attached hereto or to Paper No. _12_

☐ including changes required by the proposed drawing correction filed on _____, which has been approved by the examiner.

☐ including changes required by the attached Examiner's Amendment/Comment.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the reverse side of the drawings. The drawings should be filed as a separate paper with a transmittal letter addressed to the Official Draftperson.

☐ Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Any reply to this notice should include, in the upper right hand corner, the APPLICATION NUMBER (SERIES CODE/SERIAL NUMBER). If applicant has received a Notice of Allowance and Issue Fee Due, the ISSUE BATCH NUMBER and DATE of the NOTICE OF ALLOWANCE should also be included.

Attachment(s)

☐ Notice of References Cited, PTO-892

☑ Information Disclosure Statement(s), PTO-1449, Paper No(s). _11_

☐ Notice of Draftperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

☐ Interview Summary, PTO-413

☐ Examiner's Amendment/Comment

☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material

☐ Examiner's Statement of Reasons for Allowance

TAN T. NGUYEN
PRIMARY EXAMINER
GROUP 2800

PTOL-37 (Rev. 8/97)

*U.S. GPO: 1998-433-521/82100
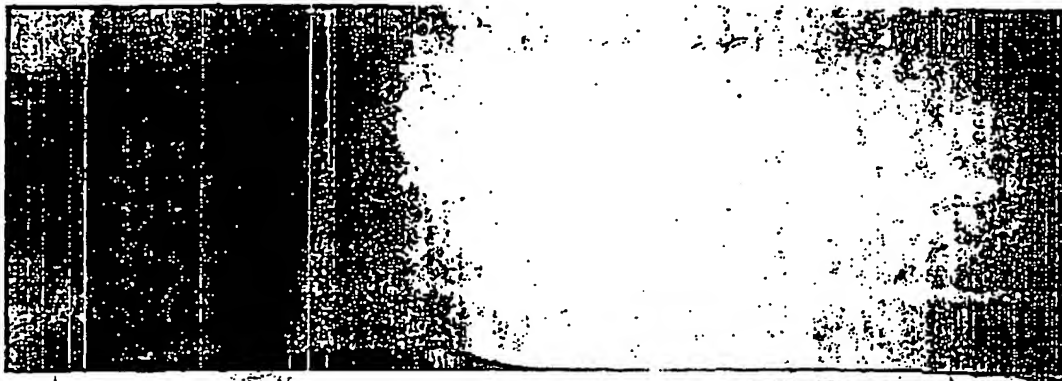
UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office

NOTICE OF ALLOWANCE AND ISSUE FEE DUE

MMC1/1128

Neil A Steinberg Esq
Rambus Inc
2465 Latham Street
Mountain View CA 94040

APPLICATION NO.	FILING DATE	TOTAL CLAIMS	EXAMINER AND GROUP ART UNIT	DATE MAILED
09/492,982	01/27/00	026	NGUYEN, T	2818

First Named Applicant	FARMWALD,	35 USC 154(b) term ext. =	0 Days

TITLE OF INVENTION	METHOD OF OPERATING A MEMORY DEVICE HAVING A VARIABLE DATA INPUT LENGTH H

ATTY'S DOCKET NO.	CLASS-SUBCLASS	BATCH NO.	APPLN. TYPE	SMALL ENTITY	FEE DUE	DATE DUE
3 P043D2C3C	365-233.000	V56	UTILITY	NO	$1240.00	02/25

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED.

THE ISSUE FEE MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED.

HOW TO RESPOND TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.
- If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is changed, pay twice the amount of the FEE DUE shown above and notify the Patent and Trademark Office of the change in status, or
B. If the status is the same, pay the FEE DUE shown above.

If the SMALL ENTITY is shown as NO:

A. Pay FEE DUE shown above, or

B. File verified statement of Small Entity Status before, or with, payment of 1/2 the FEE DUE shown above.

II. Part B-Issue Fee Transmittal should be completed and returned to the Patent and Trademark Office (PTO) with your ISSUE FEE. Even if the ISSUE FEE has already been paid by charge to deposit account, Part B Issue Fee Transmittal should be completed and returned. If you are charging the ISSUE FEE to your deposit account, section "4b" of Part B-Issue Fee Transmittal should be completed and an extra copy of the form should be submitted.

III. All communications regarding this application must give application number and batch number.
Please direct all communications prior to issuance to Box ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PATENT AND TRADEMARK OFFICE COPY

PTOL-85 (REV. 10-96) Approved for use through 06/10/99. (0651-0033)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
(Case No. P043D2C3C)

In the Application of:)
)
        FARMWALD ET AL.   )   Group:
)   Art Unit: 2818
Serial No: 09/492,982   )
)   Before
Filed: January 27, 2000   )   Examiner: T. Nguyen
)
Title: METHOD OF OPERATING A MEMORY   )
         DEVICE HAVING A VARIABLE DATA   )
         INPUT LENGTH   )

Assistant Commissioner for Patents
Washington, DC 20231

Attn.: Official Draftsperson

TRANSMITTAL OF FORMAL DRAWINGS

Dear Sir:

    Enclosed herewith is one (1) set of fourteen (14) sheets of formal
drawings for filing in the above-referenced patent application. The
changes required by Applicants' proposed drawing corrections have been
approved by the Examiner and incorporated into the attached formal
drawings.

    Applicants respectfully request that the enclosed drawings be
accepted as formal drawings in the above-referenced application.

                                        Respectfully submitted,

Date: December 9, 2000

                                        Neil A. Steinberg
                                        Reg. No. 34,735
                                        650-944-7772

PART B—ISSUE FEE TRANSMITTAL

Complete and mail this form, together with applicable fees, to:
Box ISSUE FEE
Assistant Commissioner for Patents
Washington, D.C. 20231

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MAILING INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE. Blocks 1 through 4 should be completed where appropriate. All further correspondence including the Issue Fee Receipt, the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Legibly mark-up with any corrections or use Block 1)

MMC1/1128

Neil A Steinberg Esq
Rambus Inc
2465 Latham Street
Mountain View CA 94040

OIPE
DEC 1 2 2000
PATENT & TRADEMARK OFFICE

Note: The certificate of mailing below can only be used for domestic mailings of the Issue Fee Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing.

Certificate of Mailing

I hereby certify that this Issue Fee Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Box Issue Fee address above on the date indicated below.

_____ (Depositor's name)

_____ (Signature)

_____ (Date)

APPLICATION NO.	FILING DATE	TOTAL CLAIMS	EXAMINER AND GROUP ART UNIT		DATE MAILED
09/492.982	01/27/00	026	NGUYEN. T	2818	11/28/00

First Named Applicant	FARMWALD.	35 USC 154(b) term ext. =	0 Days.

TITLE OF INVENTION: METHOD OF OPERATING A MEMORY DEVICE HAVING A VARIABLE DATA INPUT LENGTH

ATTY'S DOCKET NO.	CLASS-SUBCLASS	BATCH NO.	APPLN. TYPE	SMALL ENTITY	FEE DUE	DATE DUE
3 P043D2C3C	365-233.000	V56	UTILITY	NO	$1240.00	02/28/01

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
Use of PTO form(s) and Customer Number are recommended, but not required.

[ ] Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

[ ] "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47) attached.

2. For printing on the patent front page, list (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 *Neil A. Steinberg*

2 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)
PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. Inclusion of assignee data is only appropriate when an assignment has been previously submitted to the PTO or is being submitted under separate cover. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE *Rambus Inc.*

(B) RESIDENCE: (CITY & STATE OR COUNTRY) *Mountain View, CA*

Please check the appropriate assignee category indicated below (will not be printed on the patent)
[ ] Individual [X] Corporation or other private group entity [ ] government

4a. The following fees are enclosed (make check payable to Commissioner of Patents and Trademarks):
[X] Issue Fee
[X] Advance Order - # of Copies _____

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[X] Issue Fee
[ ] Advance Order - # of Copies _5_

The COMMISSIONER OF PATENTS AND TRADEMARKS IS requested to apply the Issue Fee to the application identified above.

(Authorized Signature) *Neil Steinberg* Reg.No. 34.735 (Date) *12-7-00*

NOTE: The Issue Fee will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the Patent and Trademark Office.

Burden Hour Statement: This form is estimated to take 0.2 hours to complete. Time will vary depending on the needs of the individual case. Any comments on the amount of time required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, D.C. 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND FEES AND THIS FORM TO: Box Issue Fee, Assistant Commissioner for Patents, Washington D.C. 20231

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PTOL-85B (REV.10-96) Approved for use through 06/30/99. OMB 0651-0033   Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
(Case No. P043D2C3C)

In the Application of:)
)
        FARMWALD ET AL.   )   Group
)   Art Unit: 2818
Serial No: 09/492,982   )
)   Before
Filed: JANUARY 27, 2000   )   Examiner: T. Nguyen
)
Title: METHOD OF OPERATING A MEMORY   )
        DEVICE HAVING A VARIABLE DATA   )
        INPUT LENGTH   )

Assistant Commissioner for Patents
Washington, DC   20231

Attn: Box Issue Fee

                TRANSMITTAL OF PAYMENT OF ISSUE FEE

Dear Sir:

        Transmitted herewith for the above-referenced application are:

[XX] Issue Fee Transmittal Form PTOL-85B.
[XX] Utility Fee: $1,240.00.
[XX] Advance Order - # of Copies _5_.
[ ] A check in the amount of _____ is attached.
[XX] The Assistant Commissioner is hereby authorized to charge
     and credit Deposit Account No. 50-0998 as described below.
     A duplicate copy of this sheet is enclosed.
                [XX] Charge the amount of $1,255.00.
                [XX] Credit any overpayment.
                [XX] Charge any additional fee required.

                                    Respectfully submitted,

Date: December 3, 2000

                                    Neil A. Steinberg
                                    Reg. No. 34,735
                                    650-944-7772

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
(Case No. RA043D2C3C)

In the Application of:

FARMWALD, ET AL.

Serial No.: 09/492,982

Filed: JANUARY 27, 2000

Title: METHOD OF OPERATING A
MEMORY DEVICE HAVING A
VARIABLE DATA INPUT LENGTH

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2818

Assistant Commissioner for Patents
Washington, DC 20231

Certificate of Mailing Under 37 CFR 1.8

I hereby certify that the attached 1) Transmittal of Formal Drawings (1 page and

14 sheets of Formal Drawings); 2) Transmittal of Payment of Issue Fee (1 page and 1

copy thereof); and 3) Issue Fee Transmittal (1 page and 1 copy thereof) is/are being

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Assistant Commissioner for Patents
Washington, D.C. 20231

MISSING 5 PAGES

on December 8, 2000.

_____
(Signature)

Michiko Sites

_____
(Print Name of Person Signing Certificate)

Ms. Michiko Sites
RAMBUS INC.
2465 Latham Street
Mountain View, California   94040

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
(Atty. Docket No. RA043D2C3C)

APPLICANT: FARMWALD ET AL.　　　　　FILED: January 27, 2000
SERIAL NO.: 09/492,982
TITLE:　　METHOD OF OPERATING A MEMORY DEVICE HAVING A
　　　　　VARIABLE DATA INPUT LENGTH

RECEIPT OF THE FOLLOWING PAPERS IS ACKNOWLEDGED

1. Issue Fee Transmittal (1 page and 1 copy thereof)
2. Transmittal of Payment of Issue Fee (1 page and 1 copy thereof)
3. Transmittal of Formal Drawings and formal drawings (1 page and 14 sheets)

DATE: DECEMBER 8, 2000　　　　　　　　　　ATTY: NAS

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
(Case No. P043D2C3C)

In the Application of:)
)
    FARMWALD et al...   )
)   Group
Serial No: 09/492,982   )   Art Unit: 2818
)
Filed: JANUARY 27, 2000   )   Before
)   Examiner: T. Nguyen
Title: METHOD OF OPERATING A MEMORY   )
        DEVICE HAVING A VARIABLE DATA   )
        INPUT LENGTH   )

Assistant Commissioner for Patents.
Washington, DC 20231

INFORMATION DISCLOSURE STATEMENT

FAX RECEIVED

JAN 3 0 2001

Dear Sir:

PETITIONS OFFICE

In compliance with the duty of disclosure set forth in 37 C.F.R. §1.56, submitted herewith is a modified Form PTO-1449, including a copy of all of the documents listed therein.

The documents listed in the PTO-1449 have been recently identified in a Notice of Opposition filed against European Patent EP 1 004 956 (Hereinafter the "OPPOSITION"). EP 1 004 956 contains claims that are similar to claims in U.S. Patent 6,034,918, the parent of the instant application. A copy of the OPPOSITION is also submitted herewith.

It is respectfully requested that the Examiner make his consideration of these references formally of record with the next Action.

Respectfully submitted,

Date: January 29, 2001

Neil A. Steinberg
Reg. No. 34,735
650-947-5325

Page -1-

Not found in USPTO file:

FORM PTO-1449

Notice of Opposition to a European Patent

To the
European Patent Office

				for EPO use only
I.	**Patent opposed**		Opp. No.	OPPO (1)
		Patent No.	EP 1 004 956 B1	
		Application No.	000101832.4	
		Date of mention of the grant in the European Patent Bulletin (Art. 97(4), 98(1) EPC)	03.01.2001	

Title of the invention:
METHOD OF OPERATING A SYNCHRONOUS MEMORY HAVING A VARIABLE DATA OUTPUT LENGTH

II.	**Proprietor of the Patent** first named in the patent specification	RAMBUS INC.

Opponent's or representative's reference (max. 15 spaces)	CST/M70815G(D1)	OREF

III.	**Opponent**		OPPO (2)
	Name	MICRON EUROPE Ltd	
	Address	Micron House Wellington Business Park Dukes Ride Crowthorne Berkshire RG45 6LS UNITED KINGDOM	
	State of residence or of principal place of business	UNITED KINGDOM	
	Telephone/Telex/Fax		
	Multiple opponents	[X] further opponents see additional sheet	

IV.	**Authorisation**		OPPO (3)
	1. Representative (Name only one representative to whom notification is to be made)		
	Name	Christopher Stephen Tunstall	
	Address of place of business	Harrison Goddard Foote Tower House Merrion Way Leeds LS2 8PA UNITED KINGDOM	
	Telephone/Telex/Fax	+44 113 290 1400	+44 113 244 2829
	Additional representative(s)	[ ] (on additional sheet/see authorisation)	OPPO (5)
	2. Employee(s) of the opponent authorised for these opposition proceedings under Art. 133(3) EPC	Name(s):	
		Zur Kasse (A) € 1226,-	
	Authorisation(s) To I./2.	[X] not considered necessary [ ] has/have been registered under No. [ ] is/are enclosed	

Notice of Opposition to a European Patent

To the
European Patent Offn

						for EPO use only

I. Patent opposed

		Opp. No.	OPPO (1)

Patent No. **EP 1 004956 B1**

Application No.

Date of mention of the grant in the European Patent Bulletin
[Art. 97(4), 98(1) EPC]

Title of the invention:

II. Proprietor of the Patent

as named in the patent specification

Opponent's or representative's reference (not 15 space)   OREF

III. Opponent   OPPO (2) | | | | | | |

Name   MICRON TECHNOLOGY ITALIA. S.R.L.

Address
Via Antonio Padnorti 3/7
Nucleo Industrial (AQ)
Building #2
67051 Avezzano (AQ) Italia
ITALY

State of residence or of principal
place of business   **ITALY**

Telephone/Telex/Fax

Multiple opponents   ☐ further opponents see additional sheet

IV. Authorisation

1. Representative
   (Name only one representative to
   whom notification is to be made)   OPPO (3) | | | | | | |

   Name

   Address of place of business

   Telephone/Telex/Fax

   Additional representative(s)   ☐ (on additional sheet/has authorisation)   OPPO (5)

2. Employee(s) of the opponent
   authorised for these opposition
   proceedings under Art. 133(3)
   EPC   Name(s):

   Authorisation(s)   ☒ not considered necessary
   ☐ has/have been registered
   under No.
   To 1./2.   ☐ is/are enclosed

2.

V. Opposition is filed against

— the patent as a whole ☒

— claim(s) No(s) | Claims 1-21

VI. Grounds for opposition:

Opposition is based on the following grounds:

(a) the subject-matter of the European patent opposed is not patentable (Art. 100(a) EPC) because.

— it is not new (Art. 52(1); 54 EPC) ☒

— it does not involve an inventive step (Art. 52(1); 56 EPC) ☒

— patentability is excluded on other grounds i. e. | Art. | ☐

(b) the patent opposed does not disclose the invention in a manner sufficiently clear and complete for it to be carried out by a person skilled in the art (Art. 100(b) EPC: see Art. 83 EPC). ☒

(c) the subject-matter of the patent opposed extends beyond the content of the application/ of the earlier application as filed (Art. 100(c) EPC. see Art. 123(2) EPC). ☒

VII. Facts and arguments
(Rule 55(c) EPC)
presented in support of the opposition are submitted herewith on a separate sheet (annex 1) ☒

VIII. Other requests:

That the Patent be revoked in its entirety.

That this opposition be subject to EXPEDITED HANDLING.

for EPO use only

Printed:05-01-2001

3

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IX. Evidence presented

Enclosed ☐
will be filed at a later date ☒

A.	Publications:	Publication date
	1 International Patent Application WO91/16680, Published October 31, 1991 ("The Parent Application")	
	Particular relevance (page, column, line, fig.):	
	See Statement of Grounds of Opposition	
	2 US Patent 4,763,249, Published August 9, 1988 ("Bomba")	
	Particular relevance (page, column, line, fig.):	
	See Statement of Grounds of Opposition	
	3 US Patent 4,394,753, Published July 19, 1983 ("Penzel")	
	Particular relevance (page, column, line, fig.):	
	See Statement of Grounds of Opposition	
	4 US Patent 4,785,428, Published November 15, 1988 ("Bajwa")	
	Particular relevance (page, column, line, fig.):	
	See Statement of Grounds of Opposition	
	5 "The Scalable Coherent Interface Project (SuperBus)", SCI-22Aug88-doc ("SCI A")	
	Particular relevance (page, column, line, fig.):	
	See Statement of Grounds of Opposition	
	6 "Scalable Coherent Interface", SCI-28Nov88-doc20 ("SCI B")	
	Particular relevance (page, column, line, fig.):	
	See Statement of Grounds of Opposition	
	7 P1596: "SCI, A Scalable Coherent Interface", SCI-28Nov88-doc 2 ("SCI C")	
	Particular relevance (page, column, line, fig.):	
	See Statement of Grounds of Opposition	
	Continued on additional sheet ☒	

B. Other evidence

Continued on additional sheet ☐

4

	for EPO use only
IX. Evidence presented Enclosed = ☐ will be filed at a later date = ☒	

A Publications:	Publication date
1 "Proposal for Clock Distribution in SCI" - 5/5/89 ("SCI D") Particular relevance (page, column, line, fig.) See Statement of Grounds of Opposition	
2 Norsk Data Report - "A Proposal for SCI Operation" by Knut Alnes - November 1988 ("SCI E") Particular relevance (page, column, line, fig.) See Statement of Grounds of Opposition	
3 "Scalable I/O Architecture for Buses" by David V. James, SCI-28Nov88-doc3 (SCI F") Particular relevance (page, column, line, fig.) See Statement of Grounds of Opposition	
4 Motorola MC88200 Cache/Memory Management Unit User's Manual, Published 1988 ("MC88200") Particular relevance (page, column, line, fig.) See Statement of Grounds of Opposition	
5 Japanese Patent Application No. S63-142445, Published June 14, 1988, and English Translation ("Teguchi") Particular relevance (page, column, line, fig.) See Statement of Grounds of Opposition	
6 US Patent 4,315,308, Published February 9, 1982 ("Jackson") Particular relevance (page, column, line, fig.) See Statement of Grounds of Opposition	
7 Japanese Patent Application Sho 62-71428, Published October 5, 1988, and English Translation ("Yamaguchi") Particular relevance (page, column, line, fig.) See Statement of Grounds of Opposition	
Continued on additional sheet ☒	

B. Other evidence	
Continued on additional sheet ☐	

IX.	Evidence presented		for EPO use only
		Enclosed = ☐	
		will be filed at a later date = ☒	

A.	Publications	Publication date
1	GigaBit Logic, 1989 GaAs IC Data Book & Designer's Guide, August 1989, 12G014, 256´4-Bit Registered Self-Timed SRAM ("GigaBit")	
	Particular relevance (page, column, line, fig.): See Statement of Grounds of Opposition	
2	US Patent No. 4,499,538, Issued February 12, 1985 ("Gemma")	
	Particular relevance (page, column, line, fig.): See Statement of Grounds of Opposition	
3	Japanese Patent Application Sho 62-185253, Published January 31, 1989, and English Translation ("Kumagai")	
	Particular relevance (page, column, line, fig.): See Statement of Grounds of Opposition	
4	UK Patent Application GB-2,197,553, Published May 18, 1988 ("Lofgren")	
	Particular relevance (page, column, line, fig.): See Statement of Grounds of Opposition	
5	IEEE Journal of Solid State Circuits, Vol. 25, No. 1, February 1990, "An On-Chip Smart Memory for a Data-Flow CPU" ("Uvieghara")	
	Particular relevance (page, column, line, fig.): See Statement of Grounds of Opposition	
6	US Patent No. 4,637,018, Issued January 13, 1987, ("Flora"), as Exemplifying Common General Knowledge.	
	Particular relevance (page, column, line, fig.): See Statement of Grounds of Opposition	
7	Japanese Patent Application JP-A-01-284132, published November 15, 1989, and English Translation ("Kosugi")	
	Particular relevance (page, column, line, fig.): See Statement of Grounds of Opposition	
	Continued on additional sheet ☒	

B.	Other evidence	
	Continued on additional sheet ☐	

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IX. Evidence presented	Enclosed ☐	
	will be filed at a later date ☒	
A. Publications:		Publication date
1 Motorola MC88200 Cache/Memory Management Unit User's Manual, Published 1988, as Exemplifying Common General Knowledge ("MC88200")		
Particular relevance (page, column, line, fig.): See Statement of Grounds of Opposition		
2 US Patent 4,680,738, Published July 14, 1987 ("Tam")		
Particular relevance (page, column, line, fig.): See Statement of Grounds of Opposition		
3 US Patent 4,330,852, Published May 18, 1982 ("Redwine")		
Particular relevance (page, column, line, fig.): See Statement of Grounds of Opposition		
4		
Particular relevance (page, column, line, fig.):		
5		
Particular relevance (page, column, line, fig.):		
6		
Particular relevance (page, column, line, fig.):		
7		
Particular relevance (page, column, line, fig.):		
Continued on additional sheet ☐		
B. Other evidence		
Continued on additional sheet ☐		

	for EPO use only
X. Payment of the opposition fee is made	
☒ as indicated in the enclosed voucher for payment of fees and costs (EPO Form 1010)	
☐	

XI. List of documents

Enclosure No.			No. of copies	
0	☒	Form for notice of opposition	2	min. 2
1	☒	Facts and arguments (see VII.)	2	min. 2
2		Copies of documents presented as evidence (see IX.)		
2a	☐	— Publications		min. 2 of each
2b	☐	— Other documents		min. 2 of each
3	☐	Signed authorisation(s) (see IV.)		
4	☒	Voucher for payment of fees and costs (see X.)	1	
5	☐	Cheque		
6	☒	Additional sheet(s)	2	min. 2 of each
7	☐	Other (please specify here)		

XII. Signature
of opponent or representative

Place   Leeds, UNITED KINGDOM

Date   January 3, 2001

Christopher Stephen Tunstall

EUROPEAN PATENT NO. 1 004 956

STATEMENT OF GROUNDS OF OPPOSITION

1. ADDED SUBJECT-MATTER ART. 76(1) EPC

    1.1.   The Patent discloses subject-matter not disclosed in the Parent Application as originally filed on two counts, namely impermissible claim broadening and impermissible intermediate claim generalisations.

    1.2.   Impermissible Claim Broadening

        1.2.1.1.   The Parent Application disclosed and claimed several different alleged inventions. It is necessary to determine to which of these the granted claims relate, otherwise the comparison required by Art. 76(1) EPC cannot be made. In total, there were 7 objectives of the invention and 21 independent claims. The interrelationships between the objectives and claims need not be explored here in full. For present purposes, it is clear that granted claim 1 is based upon PCT claim 38, this being the broadest claim to modifiable data block size transfers. This was acknowledged by the patentee in its representative's letter dated 28 January 2000, numbered para. 1. It is also clear that neither PCT claim 38 nor granted claim 1 provides any solution to the 6 original objectives that have not found their way into the Patent.

        1.2.2.   The one objective of the alleged invention as set out in the Parent Application that survived in the Patent was this.

            1.2.2.1.   "One object of the present invention is to use a new bus interface built into semiconductor devices to support high-speed access to large blocks of data from a single memory device by an external user of the data, such as a microprocessor, in an efficient and cost-effective manner" [Parent Application, 6:8-12]. This will be referred to as "objective 1."

        1.2.3.   However, one of the 6 abandoned objectives, or rather one part of a compound objective, is relevant to the present discussion as follows.

            1.2.3.1.   "Yet another objective of this invention is to provide a method for transmitting address, data and control information over a relatively narrow bus ..." [Parent Application, 6: 21-23]. This will be referred to as "objective 2."

        1.2.4.   PCT claim 38 is a dependent claim. It depends from PCT claim 28. PCT claim 28 depends from PCT claim 26. PCT claim 26 depends from PCT claim 25. PCT claim 25 is an independent claim. In these circumstances, it is not altogether surprising that PCT claim 38 can be shown not to achieve any of the 7 primary objects of the invention. That is a privilege normally reserved for independent claims rather than claims three steps lower in the hierarchy.

        1.2.5.   <u>If any objective was achieved by PCT claim 25, it was objective 2</u>

            1.2.5.1.   PCT claim 25 reads as follows.

                "25.   A bus subsystem comprising:
                two semiconductor memory devices connected in parallel to a bus, wherein one of said semiconductor devices is a master device,
                said master device including a means for initiating bus transactions,
                said bus including a plurality of bus lines for carrying substantially all address, data and control information needed by said devices,

said control information including device-select information,
said bus containing substantially fewer lines than the number of bits in a single address, and
said bus carrying device-select information without the need for separate device-select lines connected directly to individual devices on said bus, whereby said master device initiates bus transactions which transfer information between said semiconductor devices on said bus."

1.2.5.2.   This claim clearly relates to a bus subsystem. The bus includes a plurality of bus lines for carrying substantially all address, data and control information needed by the device for communication with substantially every other device connected to the bus, and has substantially fewer bus lines than the number of bits in a single address. A bus including a plurality of such general purpose lines, each carrying in a time-multiplexed manner substantially all address, data and control information needed by the device for communication with substantially every other device connected to the bus, and having substantially fewer bus lines than the number of bits in a single address, will be referred to in the present document as a "highly multiplexed bus." That the Parent Application was concerned with such a bus is constantly reinforced throughout the Parent Application including the summary of the invention and the beginning of the specific description [Parent Application, 7:10-19; 7:25-8:2; 11:16-25]. In addition, the bus subsystem of PCT claim 25 requires device selection to be accomplished using the control information carried by the bus.

1.2.5.3.   The bus is clearly a "relatively narrow bus" as required by objective 2. It is explicitly said to contain "substantially fewer bus lines than the number of bits in a single address." The operation of the bus subsystem of claim 25, with the master device initiating bus transactions over a bus that carries substantially all address, data and control information needed by the devices and contains substantially fewer lines than the number of bits in a single address, amounts to a "method for transmitting address, data and control information over a relatively narrow bus ..." as required by objective 2.

1.2.6.   Objective 1 was not achieved by PCT claim 25 .

1.2.6.1.   Objective 1 concerns "high-speed access to large blocks of data from a single memory device ... in an efficient and cost-effective manner." PCT claim 25 makes no reference to the transfer of large blocks of data, nor indeed of blocks of data of any size. Nor does it make reference to memory devices. It contains no integers that in any way determine the ability of the bus subsystem to achieve objective 1. Whether or not the bus subsystem of claim 25 can meet objective 1 depends upon matters that do not form the subject of claim 25. These matters include the measures described in "DRAM Column Access Modification" [Parent Application, 59:4-62:2]. These measures quite clearly concern a "bus interface built into semiconductor devices." They include internal I/O multiplexing, allowing the interfacing of a memory device running at a relatively slow internal clock rate with the high-speed bus of the alleged invention [Parent Application, 60:1-6]. This increases the bandwidth of DRAM access [Parent Application, 59:19-2; 61:3-13]. It was acknowledged that the invention lay not in these measures per se, but in their use with the high-speed highly multiplexed bus of the invention [Parent Application 59:23-25]. These measures were the subject-matter of claims 82-90 and 114-123 of the Parent Application. This fits into the expected scheme of things: a number of these claims are independent.

1.2.6.2.   As has been shown, if any of the primary objectives of the invention was achieved by PCT claim 25, it was objective 2. It is hardly surprising that objective 1 was not achieved by this claim. One would not normally expect a

single independent claim to achieve two distinct and unrelated primary objectives of the invention.

1.2.7. Objective 1 was not achieved by PCT claim 26

1.2.7.1. PCT Claim 26 restricts PCT claim 25 to the case of a memory device connected to the bus, having one or more discrete memory sections and a modifiable address register to store memory address information which corresponds to the one, or each, discrete memory section. The bus is an integer of PCT claim 25. Whilst PCT claim 26 mentions a memory device, it says nothing that concerns "high-speed access to large blocks of data" from the memory device "in an efficient and cost-effective manner."

1.2.8. Objective 1 was not achieved by PCT claim 28

1.2.8.1. PCT claim 28 restricts PCT claim 26 to packet-based split-cycle transactions, in which the request packet from the bus master includes address and control information. The address information points to at least one memory location within a discrete memory section of the memory device. The memory section and memory device are integers of PCT claim 26. The control information includes information about the requested bus transaction and about the access time (corresponding to a number of bus cycles that need to intervene before bus access begins). PCT claim 28 says nothing that concerns "high-speed access to large blocks of data" from the memory device "in an efficient and cost-effective manner."

1.2.8.2. In relation to access times, an integer of PCT claim 28, there are few references in the Parent Application. One reference however reads as follows.

> "A request packet and the corresponding bus access are separated by a selected number of bus cycles, allowing the bus to be used in the intervening bus cycles by the same or other masters for additional requests or brief bus accesses. Thus multiple, independent accesses are permitted, allowing maximum utilisation of the bus for transfer of short blocks of data. Transfers of long blocks of data use the bus efficiently even without overlap because the overhead due to bus address, control and access times is small compared to the total time to request and transfer the block" [Parent Application, 15:23-16:7].

1.2.8.3. This passage is a very clear statement of the advantages of modifiable access times. In the transfer of short blocks of data, modifiable access times allow for interleaving of requests and thus greater efficiency. In the transfer of long blocks of data, the need to transfer access time information on the bus is an overhead. It reduces efficiency. There is no possibility of interleaving long block requests. The preferred embodiments described in the Parent Application do not allow it. However, this overhead is an acceptable efficiency reduction because, compared with the overall length of the transaction, the overhead is small.

1.2.8.4. Objective 1 concerns "high-speed access to large blocks of data ... in an efficient and cost-effective manner." Modifiable access times contribute nothing to the achievement of that objective; as acknowledged in the Parent Application itself, they detract from it. PCT claim 28 frustrates this objective.

1.2.9. Objective 1 was not achieved by PCT claim 38

1.2.9.1. PCT claim 38 restricts PCT claim 28 to situations in which the control information includes a block-size value that encodes and specifies the size of

the block of data to be transferred. The control information is an integer of
PCT claim 28. Here at last, in a thrice dependent claim, an afterthought to an
afterthought to an afterthought, is a reference to the transfer of a block of
data. Claim 38 does not require that the size of the data block be large. The
claim says nothing about whether the block is small or large. Moreover,
claim 38 merely states that the size of the data block to be transferred is
specified in the transaction request packet. It says nothing that determines
whether the data block transfer is high-speed, efficient or cost effective,
merely that its size can be determined. As discussed above, the answers to
these questions lie in subject-matter that is entirely absent from the claim and
is to be found in PCT claims 82-90 and 114-123.

1.2.10. To summarise, the granted claims find their basis in thrice dependent PCT claim 38.
Independent PCT claim 25 from which PCT claim 38 ultimately depends, achieves
(if anything) objective 2 and does not achieve objective 1. Objective 1 is not
achieved by PCT claims 25 or 38 or any intervening claim, but is achieved by
wholly different claims with wholly different subject-matter. PCT claim 38 and
granted claim 1 achieve none of the primary objectives of the alleged invention.

1.2.11. **The Technical Board of Appeal case law on claim broadening is settled.**

1.2.11.1. The test for whether claim broadening is contrary to Art. 123(2) EPC, and
therefore Art. 76(1) EPC also, was clearly enunciated in decision T331/87,
following decisions T194/84 and T260/85. The test was approved in decision
T514/88 and is threefold [T331/87, Reasons 6].

1.2.11.2. "The removal of an integer from a claim may not violate Art. 123(2) EPC
provided the skilled reader would directly and unambiguously recognise that:

1.   the integer was not explained as essential in the original disclosure;

2.   it is not, as such, indispensable for the function of the invention in
the light of the technical problem it serves to solve; and

3.   the replacement or removal requires no real modification of other
integers to compensate for the change."

1.2.12. **Granted claim 1 lacks an essential element of the alleged invention as originally
disclosed.**

1.2.12.1. Granted claim 1 relates to a method of operating a semiconductor memory
device that includes, "... receiving block size information wherein the block
size information defines an amount of data to be output onto an external bus
in response to a read request; and outputting the amount of data ... in
response to a read request ..." PCT claim 38, through its thrice dependent
structure, explicitly required the bus to be a highly multiplexed bus. Granted
claim 1, if it no longer contains this implied requirement, is broader than
PCT claim 38. Such broadening is inadmissible.

1.2.12.2. Was the highly multiplexed bus explained as essential in the original
disclosure?

1.2.12.2.1. According to decisions T260/85 and T527/88, in determining what is
explained or disclosed in the application, it is necessary to read the
document as a whole and individual passages within it in context. In
view of this, a line-by-line analysis is no substitute for gaining an
overall impression of the document by reading it from start to finish.
However, the following points are mentioned to give a flavour for the
disclosure of the Parent Application.

1.2.12.2.1.1. The Parent Application was entitled "Integrated Circuit I/O Using a High Performance Bus Interface".

1.2.12.2.1.2. The discussion of the prior art drew many distinctions between the numerous documents mentioned and the alleged invention, some of which were applicable to different alleged inventions from those originally claimed. However, in every case bar one, the documents were distinguished from the invention on the basis that it did not possess features of the bus interface [Parent Application, 3:14-18; 3:25-4:3; 4:5-7; 4:13-14; 4:16-18; 5:13-14; 6:5-7]. The single exception was a reference that described a clocking scheme that was distinguished from the clocking scheme used in the invention [Parent Application, 5:19-25]. The claims in the Parent Application that were directed to the clocking scheme, claims 73-81, and those directed to the chip package, claims 91-94, were the only claims not limited to the highly multiplexed bus.

1.2.12.2.1.3. Moreover, the state of the art was summed up thus: "None of the buses described in patents or other literature use only bused connections. All contain some point-to-point connections on the backplane" [Parent Application 5:13-15].

1.2.12.2.1.4. The summary of the invention opens with a discussion of the highly multiplexed bus [Parent Application, 7:10-19]. The necessary modifications that conventional DRAMs must undergo to comply with the alleged invention is described [Parent Application, 8:9-9:7] These modifications concern the interface with the highly multiplexed bus.

1.2.12.2.1.5. The objective achieved by PCT claim 38 via its dependency upon PCT claim 25, was concerned with the highly multiplexed bus. This is highly relevant [T514/88].

1.2.12.2.1.6. The entire specific description is concerned with a highly multiplexed bus [cf. Parent Application, 11:16-12:10].

1.2.12.2.1.7. All of the original claims, apart from those directed to the clocking and packaging schemes, were limited to the highly multiplexed bus.

1.2.12.2.2 All of these matters point to the essentiality of the highly multiplexed bus. Indeed, the whole tenor of the Parent Application was that it concerned a new bus architecture. There is no disclosure, suggestion or implication that anything else was contemplated. It is what the inventors contemplated, as objectively determined from their original application, that counts [T260/85, Reasons:10]. The Parent Application clearly explained that the highly multiplexed bus was an essential element of the alleged invention of PCT claim 38. No other reading or explanation is possible.

1.2.12.3. Was the highly multiplexed bus, as such, indispensable for the function of the invention in the light of the technical problem it serves to solve?

1.2.12.3.1. This is a straightforward question to answer. The technical problem that PCT claim 38 served to solve, via its dependency upon PCT claim 25, was to provide "a method for transmitting address, data and control information over a relatively narrow bus ..." [Parent Application, 6: 21-23]. The only relatively narrow bus disclosed is the highly multiplexed bus. In this context, it is noteworthy that the acknowledged prior art

included buses in which the address information was multiplexed [Parent Application, 4:15-20]. It also included buses in which data and address information was multiplexed on the same lines [Parent Application, 4:21-23]. In each case, some control signals were bused. In distinguishing the alleged invention from the prior art by requiring "address, control and data" information to be transmitted on a "relatively narrow" bus, objective 2 can only have meant the highly multiplexed bus disclosed. Therefore, compatibility with the highly multiplexed bus was not just indispensable; it was a prerequisite.

1.2.12.3.2   Moreover, not only was the objective to be achieved expressly stated to concern compatibility with the highly multiplexed bus, but also any performance advantages attributable to modifiable block size transactions are present only in the context of the highly multiplexed bus.

1.2.12.4.   Would the removal of the requirement for the highly multiplexed bus require any real modification of other integers to compensate for the change?

1.2.12.4.1.   Again, this is a straightforward question to answer. Removal of this requirement has far-reaching consequences.

1.2.12.4.2   Firstly, the bus interface circuits of the semiconductor devices would no longer need to allow it to demultiplex and decode relevant bus transactions. They require modification.

1.2.12.4.3.   Secondly, the nature of the "request packet" of PCT claim 38, via its dependency on PCT claim 28, is defined by the highly multiplexed nature of the bus. Removal of this interdependence would be a radical departure from the teaching of the application as filed, in which requests had to be encoded and multiplexed onto the bus lines in the way shown in and described with reference to Fig. 4 of the Parent Application [Parent Application, 21:21-24:2]. Any removal of the requirement for the highly multiplexed bus would radically alter the meaning of the term "request" as between PCT claim 38 and granted claim 1.

1.2.12.4.4.   Thirdly, as discussed, modifiable block size transactions are disclosed only in the context of the highly multiplexed bus and do not in the inventors' view have an existence independent of it. Any removal of the requirement for the highly multiplexed bus would also remove the justification for modifiable block size transactions as perceived by the inventors.

1.2.12.5.   For all these reasons, if the requirement in PCT claim 38 for the highly multiplexed bus is absent from granted claim 1, its absence fails all three limbs of the test established by the Technical Board of Appeal. It would amount to inadmissible claim broadening contrary to Art. 123(2) EPC, and therefore Art. 76(1) EPC also.

1.2.13.   Granted claim 1 lacks further essential elements of the invention as originally disclosed.

1.2.13.1.   Apart from the highly-multiplexed bus, granted claim 1 makes no explicit reference to a plethora of other integers of PCT claim 38. These include the following.

1.2.13.1.1.   The reference in PCT claim 25 to the bus carrying device-select information without the need for separate device-select lines is not explicitly recited.

1.2.13.1.2. The reference in PCT Claim 26 to the memory device having a modifiable address register to store memory address information corresponding to one or more discrete memory sections is not explicitly recited.

1.2.13.1.3. The reference in PCT claim 28 to packet-based split-cycle transactions is not explicitly recited.

1.2.13.1.4. The reference in PCT claim 28 to the transaction request packets including address and control information is not explicitly recited.

1.2.13.1.5. The reference in PCT claim 28 to the control information of the request packet including information about the access time (corresponding to a number of bus cycles to intervene before bus access begins) is not explicitly recited.

1.2.13.1.6. The reference in PCT claim 38 to the control information of the request packet including the block-size value is not explicitly recited.

1.2.13.2. If these requirements of PCT claim 38 are missing from granted claim 1, then these omissions are inadmissible. All the integers omitted were present in the embodiments described. They could each be discussed in isolation, but it is more informative to look at the overall picture. In effect, claim 25 of the Parent Application has been rewritten as a method claim (to avoid having to mention the bus master) and then relieved of its very essence, namely the requirements for the highly multiplexed bus and for the bus to carry device select information. Into this wholly emasculated claim have been introduced a series of isolated integers including all of the three method steps of granted claim 1, none of which relate to the objective originally achieved by PCT claim 25. Clearly, it is not permissible for the patentee to remove from claim 25 the very integers that allow it to achieve the objective that the inventors had in mind for it. It amounts to abandoning the claim and reconstructing, ex post facto, a new claim including a selection of integers isolated from the original disclosure, whether from the claims or the description or the claims, irrespective of their relevance to the original primary objectives of the invention. That is not allowed.

1.2.13.3. Even if such an approach were admissible in principle, which the decisions of the Technical Board of Appeal cited above clearly demonstrate not to be the case, granted claim 1 contains impermissible intermediate generalisations, as will be discussed in the following section.

1.3. Impermissible Intermediate Generalisation

1.3.1. The Technical Board of Appeal case law on intermediate generalisation is settled.

1.3.1.1. The test for whether intermediate generalisation is contrary to Art. 123(2) EPC, and therefore Art. 76(1) EPC also, was clearly enunciated in decision T284/94, following decision T17/86.

1.3.1.2. "An amendment of a claim by the introduction of a technical feature taken in isolation from the description of a specific embodiment is not allowable under Art. 123(2) EPC if it is not clear beyond any doubt for a skilled reader from the application documents as filed that the subject-matter of the claim thus amended provides a complete solution to a technical problem unambiguously recognisable from the application."

1.3.1.3. A number of other passages from this decision shed useful light on how this test is to be applied, in particular the following statements.

1.3.1.3.1. Referring to T17/86, an isolated technical feature "may be introduced into a claim without contravening Art. 123(2) EPC, provided that it is "'evident beyond doubt to a skilled person reading the description that this isolated technical feature on its own enables the object in view to be achieved'" " (T284/94, Reasons point 2.13, para. 2).

1.3.1.3.2. "In following this decision, the object to be achieved by the subject-matter of the amended claim has to be established as well as whether the claims define all means necessary for achieving this object" [T284/94, Reasons point 2.1.4, para. 1].

1.3.1.3.3. "Because of the fact that features disclosed in the context of a specific embodiment and added to a claim may achieve in an unambiguously recognisable manner an object different from that present in the introductory part of a description, it should further be ascertained whether such a further object is disclosed and whether it is clear beyond doubt for a skilled person reading the application as filed that the added technical features on their own achieve this further object" [T284/94, Reasons point 2.1.4, para. 3]. This makes clear the important distinction between objects that are relevant to claim broadening, i.e. the original objectives of the invention set out as such, and objects relevant to intermediate generalisation, which can be derived from other parts of the application, but only to the extent they are disclosed.

1.3.2 **Granted claim 1 includes a technical feature that has been isolated from its original context and does not provide a complete solution to any technical problem disclosed in the Parent Application.**

1.3.2.1. PCT claim 38 required the block-size value to be included in control information that, together with address information, is bundled into a single request. That is exactly what is described in the Parent Application with reference to Fig. 4 [Parent Application, 21:21-22:10, esp. 22:9-10; 27:23-30]. No advantage is ascribed in the Parent Application to the subject matter of PCT claim 38, as distinct from the subject matter of the claims from which it depends.

1.3.2.2. Granted claim 1 contains no explicit requirement for the block size value to be included with address information in a transaction request.

1.3.2.3. As stated above, no advantage is ascribed in the Parent Application to the subject matter of PCT claim 38, as distinct from the subject matter of the claims from which it depends. This is a crucial point. According to the test established by the Technical Board of Appeal for admissibility of intermediate generalisation, it can only be justified if there is an advantage – a solution to a technical problem – disclosed in the Parent Application that is completely solved by the intermediate generalisation. If there is no problem and no solution, no advantage disclosed, the generalisation must fail. Such is the case here.

1.3.2.4. In spite of the above, it is not difficult to understand the purpose of PCT claim 38 in the context of a system where high-speed access to blocks of data is desired, and in which all bus transaction requests are six bus cycles long. It would be foolish to require one bus transaction to establish a block size and a second bus transaction to make the block transfer request. This would only increase the block request overhead to which the Parent Application refers [Parent Application, 15:23-16:7]. This purpose, namely allowing block size selection with no additional overhead, was not disclosed as such, but if it had been, it would not assist the patentee: it is only achieved by integrating the block size value into the transaction request, which explains why the inventors took such pains to allow both very small block sizes (block size 1)

and very large block sizes (block size 1024) to be represented by binary encoding using only four bits (Parent Application, 28:1-11]. It also explains the use of the word "encodes" in addition to "specifies" in PCT claim 38. Unless the block size value is so integrated, bus overhead will increase.

1.3.2.5.   For this reason, if granted claim 1 does not require that block size information be integrated into a transaction request, then the claim fails the test established by the Technical Board of Appeal. It amounts to inadmissible intermediate generalisation contrary to Art. 123(2) EPC, and therefore Art. 76(1) EPC also.

1.3.2.6.   It is worthy of note that it is not enough in the present context to say that the advantage or purpose of PCT claim 38 is to allow block size selection; that is tautologous. It amounts to saying that the advantage of an integer is its own existence; the problem to be solved by an integer its own provision. On that basis, every intermediate generalisation could be justified; but that is not the law.

1.3.3.   Granted claim 1 includes a further technical feature that has been isolated from its original context and does not provide a complete solution to any technical problem disclosed in the Parent Application.

1.3.3.1.   PCT claim 38, via its dependency on PCT claim 28, specifies, "... a means for said master device to request said memory device to prepare for a bus transaction by sending a request packet along said bus ..." PCT claim 28 and PCT claim 38 then go on to specify the information contained within the request packet. Clearly, PCT claims 28 and 38 define in general terms a bus transaction protocol. As such, it is applicable to all bus transactions. Accordingly, every bus transaction is initiated by the master device requesting the memory device to prepare for a bus transaction by sending a request packet along the bus, the request packet including the specified information. This applies as much to write transaction requests as it does to read transaction requests. This is consistent with the preferred embodiment of the invention, in which exactly the same form of transaction request, as shown in Fig. 4, is used to request read or write block transfers. The only difference is one bit identifying whether the transaction is a read or a write transaction [Parent Application, 22:19-23:3].

1.3.3.2.   Notably, according to claim 28, and therefore claim 38 also, the request packet should contain access time information (corresponding to a number of bus cycles to intervene before bus access begins). As discussed, the technical problem solved by modifiable access times, as claimed in PCT claim 103, was to maximise bus utilisation for exchange of small blocks of data in a highly multiplexed system [Parent Application, 16:1-3]. Modifiable access time DRAM read operations were discussed in the Parent Application in conjunction with modifiable access time DRAM write operations. Whereas bus utilisation may be improved by providing for modifiable access times in respect of read operations only, it is not a complete solution to the problem of maximising bus utilisation. For the achievement of that objective, the device must have programmable access times in respect of all operations that require it to utilise the bus in response to a request. This underlines the fact that PCT claim 38 was for good reason not limited to a particular type of transaction request.

1.3.3.3.   Granted claim 1 relates to a method in which a semiconductor memory device responds in a certain way to read requests only. If granted claim 1 were limited to the operation of read only devices such as ROMs, this limitation to read requests only would not be objectionable. However, granted claim 1 also covers the operation of read/write devices such as

RAMs that receive block-size values for use in read requests only, and not in write requests. This represents an impermissible intermediate generalisation.

1.3.3.4.   As has already been mentioned, no technical problem that is disclosed in the Parent Application is solved by the subject matter of claim 38. According to the test established by the Technical Board of Appeal for admissibility of intermediate generalisation, it can only be justified if there is an advantage – a solution to a technical problem – disclosed in the Parent Application that is completely solved by the intermediate generalisation. If there is no problem and no solution, no advantage disclosed, the generalisation must fail. Such is the case here.

1.3.3.5.   Even if the purpose behind PCT claim 38 as discussed above had been disclosed, the position would be no different. The purpose is to allow block size selection with no additional overhead. That applies just as much to write block size selection as to read block size selection.

1.3.3.6.   For this reason, the introduction into granted claim 1 of the requirement for block size information in respect of read operations only fails the test established by the Technical Board of Appeal. It amounts to inadmissible intermediate generalisation contrary to Art. 123(2) EPC, and therefore Art. 76(1) EPC also.

1.3.4.   Granted claim 3 includes a technical feature that has been isolated from its original context and does not provide a complete solution to any technical problem disclosed in the Parent Application.

1.3.4.1.   Granted claim 3 introduces into granted claim 1 the requirement for access time information that is found in PCT claim 28 or PCT claim 103. As discussed above, PCT claim 28 specifies information contained within a request packet. It defines in general terms a bus transaction protocol. As such, it is applicable to all bus transactions. Accordingly, every bus transaction is initiated by the master device requesting the memory device to prepare for a bus transaction by sending a request packet along the bus, the request packet including the specified information, in particular access time information, irrespective of whether it is a read or a write request. This is consistent with the preferred embodiment of the invention in which exactly the same form of transaction request, as shown in Fig. 4, is used to request read or write block transfers and includes access time information (Parent Application, 27:1-15). This type of read request access time information points to one of two access time registers that have been set up in advance

1.3.4.2.   On the other hand, according to PCT claim 103, "data may be transmitted to said [access time] register via said bus which establishes a predetermined amount of time that said semiconductor device thereafter must wait before using said bus in response to a request." This is more akin to the subject matter of granted claim 4, but as claim 4 depends from claim 3, it is relevant to claim 3 also. This type of access time information is what is put into the access time registers in the first place. It is clear from the language of PCT claim 103 that it is speaking of access time registers being set up prior to a request being made. This is consistent with the preferred embodiment of the invention, in which two access time registers are set up in advance. It is also clear from the language of PCT claim 103, in particular the phrase "thereafter must wait ... in response to a request," that it applies to all subsequent requests. This is also consistent with the preferred embodiment, in which transaction requests point to one of the two access time registers in all cases [Parent Application, 27:1-15].

1.3.4.3.   This disclosure of access time information applying in all case to both read and write transactions can easily be understood. The advantage of a

modifiable access time register is, as discussed above, to allow "maximum utilisation of the bus for transfer of short blocks of data" [Parent Application, 15:1-3]. Maximum utilisation of the bus can only be achieved if all the devices connected to the bus use a programmable access time register to time their response to all requests directed to them.

1.3.4.4.   Granted claim 3 requires the semiconductor memory device to respond in accordance with the access time information to read requests only. If granted claim 1 were limited to read only devices such as ROMs, this limitation to read requests only would not be objectionable. However, granted claim 1 also covers read/write devices such as RAMs that have programmable access times for read requests only, and not for write requests. This represents an impermissible intermediate generalisation.

1.3.4.5.   As discussed above, the technical problem solved by modifiable access times, as claimed in PCT claims 28 and 103, was to maximise bus utilisation for exchange of small blocks of data in a highly multiplexed system [Parent Application, 16:1-3]. Modifiable access time DRAM read operations were discussed in the Parent Application in conjunction with modifiable access time DRAM write operations. Whereas bus utilisation may be improved by providing for modifiable access times in respect of read operations only, it is not a complete solution to the problem of maximising bus utilisation. For the achievement of that objective, the device must have programmable access times in respect of all operations that require it to utilise the bus in response to a request. Granted claim 3 is not so limited.

1.3.4.6.   For this reason, the introduction into granted claim 3 of the requirement for modifiable access times in respect of read requests only fails the test established by the Technical Board of Appeal. It amounts to inadmissible intermediate generalisation contrary to Art. 123(2) EPC, and therefore Art. 76(1) EPC also.

1.3.5.   Granted claims 14 and 16 include a technical feature that has been isolated from its original context and does not provide a complete solution to any technical problem disclosed in the Parent Application.

1.3.5.1.   Claims 14 and 16 of the patent require internal clock signals to be generated by "a delay locked loop". The term "delay locked loop" was never used in the Parent Application. It is a wholly new term. No delay locked loop was ever disclosed. The nearest thing to it was probably to be found somewhere in the circuit illustrated in Fig. 12 of the Parent Application. The broadest disclosure of that circuit in the Parent Application is to be found in claims 78 and 108, but these claims make no mention of anything that could be regarded as a delay locked loop. The broadest disclosure in the Parent Application of any sufficiently concrete functional detail of the circuit of Fig. 12 is to be found in claim 79.

1.3.5.2.   Clearly, the object to be achieved by the circuit of Fig. 12 was to generate an internal clock signal synchronised to a time half way between the early and late bus clock signals [Parent Application, 46:20-47:1; 47:21-48:3]. This objective is only achieved if the integers of claim 79 of the Parent Application are present. Granted claims 14 and 16 are not so limited.

1.3.5.3.   For this reason, the introduction into granted claims 14 and 16 of a delay locked loop in isolation fails the test established by the Technical Board of Appeal. It amounts to inadmissible intermediate generalisation contrary to Art. 123(2) EPC, and therefore Art. 76(1) EPC also.

2. ENTITLEMENT TO DIVISIONAL STATUS

2.1. For precisely the reasons discussed above and because the objectionable added subject matter was present in the Divisional Application as filed (a fundamental error), it follows that the Divisional Application and the Patent are not entitled to the benefit of the filing and priority dates of their Parent Application. They take as their filing and priority dates the date on which it was actually filed, namely January 29, 2000. No subsequent amendment can affect the position under Art. 76(1) EPC, as indicated in decision T873/94, Reasons, Section 1, Para. 4.

3. LACK OF NOVELTY ART. 54 EPC

3.1. Each and every claim of the Patent, having a priority date of January 29, 2000, lacks novelty.

3.2. WO91/16680 ("The Parent Application"), published October 31, 1991

3.2.1. The Parent Application discloses every feature disclosed in the Patent, including all the integers of every claim.

3.3. The matter disclosed in the Parent Application does not support any claim purporting to cover buses other than the highly multiplexed bus described or read requests other than read request packets. In proceedings brought in the UK, France and Germany under the patent arising from the Parent Application, the patentee has asserted that the terms "external bus" and "request" in granted claim 1 of that patent should be afforded an interpretation wider than that supported by the Parent Application. The following discussion assumes that such a wider interpretation may be advanced by the patentee in respect of the Patent.

3.4. The subject-matter of claims 1-5, 8-10, 12-15, and 17-21 of the Patent lacks novelty even if entitled to the declared priority date of April 18, 1990.

3.5. US Patent 4,763,249, Published August 9, 1988 ("Bomba")

3.5.1. Bomba discloses a system that includes a plurality of bus devices interconnected by a synchronous, multiplexed bus. The bus device can be constructed as a memory device with a plurality of storage locations and interconnection circuitry [Bomba, abstract]. The interconnection circuitry forms an integral part of the memory device [Bomba, 6:63-65]. Thus, Bomba discloses a "semiconductor memory device having at least one memory array which includes a plurality of memory cells" and its method of operation.

3.5.2. A master clock 144 connected to the communications path generates clocking signals (time and phase signals) for the bus devices [Bomba, 9:14-32 and Figs. 3A and 3B]. These signals are received by, inter alia, the interconnection circuitry of the memory device. Thus, Bomba discloses "receiving [in the memory device] an external clock signal having a fixed frequency."

3.5.3. A two-bit data length code is placed on the highest bits of data lines D[31:30] during a command/address cycle of a read transaction [Bomba, 13:59-14:4 and Fig. 4A]. The lower 30 bits contain the device "address" (the address is the 30 bit storage location where the transaction is to take place) [Bomba, 13:59-14:4 and 14:13-15]. The data length code specifies the length of the data transfer that is to take place, e.g. one to four cycles of 32 bit data [Bomba, 15:15-28]. The operation code for the read command is transmitted over information lines I[3:0] at the same time [Bomba, 13:59-61]. As can be seen from Figs. 1A, 2 and 3B of Bomba, each of these signal is received by, inter alia, the interconnection circuitry of the memory. Thus, Bomba discloses "receiving block size information, wherein the block size information defines an amount of data to be output onto an external bus in response to a read request."

3.5.4. A memory device on the bus, containing the relevant address, confirms receipt of the command/address cycle and may begin the data transaction [Bomba, 15:49-63]. The memory device outputs data on the data lines D[31:0] during a first data cycle. The memory device continues to output new data for as many data cycles as are specified during the command/address cycle [Bomba, 15:29-16:58]. Thus, Bomba discloses "outputting the amount of data corresponding to the block size information, in response to a read request." Data is generally placed on the data lines at the leading edge of internal clock TCLK [Bomba, 9:51-54]. TCLK is the transmitting clock generated locally in the memory device from the time and phase components of master clock 144 [Bomba, 8:46-63 and 9:27-39 and Fig. 3B]. Thus, the data is output "synchronously with respect to the external clock signal."

3.5.5. It follows that the subject-matter of claim 1 is not new.

3.5.6. The memory device outputs data on the data lines D[31:0] during a first data cycle. The memory device continues to output new data for as many data cycles as are specified during the command/address cycle [Bomba, 15:29-16:58]. The time between successive TCLK signals defines a cycle [Bomba, 9:40-41]. TCLK is generated locally in the memory device from the time and phase components of master clock 144 [Bomba, 8:46-63 and 9:27-39 and Fig. 3B]. Thus, Bomba discloses that "the amount of data corresponding to the block size information is output synchronously during a plurality of clock cycles of the external clock signal."

3.5.7. It follows that the subject-matter of claim 2 is not new.

3.5.8. Data is placed on the data lines at the leading edge of TCLK [Bomba, 9:51-54]. As stated above, TCLK is generated locally from the time and phase components of Master Clock 144. Fig. 3A of Bomba shows the correlation between TCLK and the external clock signals TIME (+) and PHASE (+). A rising edge of TCLK corresponds with a next rising edge of TIME (+) after a rising edge of PHASE (+). Thus, Bomba discloses that "data is output onto the external bus synchronously with respect to a rising edge transition of the external clock signal."

3.5.9. It follows that the subject-matter of claim 8 is not new.

3.5.10. Fig. 3A of Bomba also shows the correlation between TCLK and the external clock signals TIME (-) and PHASE (-). A rising edge of TCLK corresponds with a next falling edge of TIME (-) after a falling edge of PHASE (-). Thus, Bomba discloses that "data is output onto the external bus synchronously with respect to a falling edge transition of the external clock signal."

3.5.11. It follows that the subject-matter of claim 9 is not new.

3.5.12. Bomba discloses the use of two bits to represent the length of 4 different block sizes [Bomba, 15:18-24]. Thus, the two bits are a binary representation of the block size in units of 32 bits. Therefore, Bomba discloses that "the block size information is a binary representation of the amount of data to be output after receipt of a read request."

3.5.13. It follows that the subject-matter of claim 10 is not new.

3.5.14. As discussed above, a two-bit data length code is placed on the highest bits of data lines D[31:30] during a command/address cycle of a read transaction [Bomba, 13:59-14:4 and Fig. 4A]. The lower 30 bits contain the device "address" [Bomba, 13:59-14:4 and 14:13-15]. The operation code for the read command is transmitted over information lines I[3:0] at the same time [Bomba, 13:59-61].

3.5.15. It follows that the subject-matter of claim 12 is not new.

3.5.16.   As stated above, the first internal clock signal TCLK is generated locally in each device on the bus using the master clock 144 [Bomba, 8:54-63]. Data is placed on the data lines at the leading edge of TCLK [Bomba, 9:31-34]. Thus, Bomba discloses "generating a first internal clock signal using the external clock signal wherein the amount of data corresponding to the block size information is output on to the external bus synchronously with respect to the first internal clock signal."

3.5.17.   It follows that the subject-matter of claim 13 is not new.

3.5.18.   Each memory device contains a large number of configuration registers (200-216). One such register is a control and status register 202 illustrated in Fig. 7C, that contains, inter alia, device ID information that is loaded into bits CSR[3:0] on system power-up or during a subsequent initialisation sequence [Bomba, 22:29-36]. Thus, Bomba discloses "a programmable identification register [in the memory device] to store an identification value to identify the memory device from a plurality of other memory devices on the external bus."

3.5.19.   Device ID information is transmitted as part of a read transaction received by the memory device [Bomba, 8:23-24]. It forms a part of the thirty bit device address transmitted on lines D[29:0] [Bomba, 14:13-18]. Thus Bomba discloses "receiving [in the memory device] identification information."

3.5.20.   Only the memory device addressed by the device address responds to the read transaction. The memory device compares its device ID with the ID information transmitted with the device address on lines D[29:0] and responds only if there is a match. Thus, Bomba discloses "determining whether the identification information corresponds to the identification value stored in the programmable identification register wherein, when the identification information corresponds to the identification value, the amount of data corresponding to the block size information is output onto the external bus synchronously with respect to the external clock signal."

3.5.21.   It follows that the subject-matter of claim 17 is not new.

3.5.22.   As stated above, the device ID information is loaded into bits CSR[3:0] on system power-up or during a subsequent initialisation sequence [Bomba, 22:29-36]. Thus Bomba discloses that "the programmable identification register is programmed" either "after power is applied to the memory device during an initialisation sequence" or "during an initialisation sequence of the memory device."

3.5.23.   It follows that the subject-matter of claims 19 and 20 is not new.

3.6.   US Patent 4,394,753, Published July 19, 1983 ("Penzel")

3.6.1.   Penzel describes a highly integrated memory module. As illustrated in Fig. 1 of Penzel, the highly integrated memory module is a semiconductor memory device that includes a memory cell array (DECODER MEMORY) arranged as a plurality of rows and columns [Penzel, 2:45-53]. Thus, Penzel discloses a "semiconductor memory device having at least one memory array which includes a plurality of memory cells" and its method of operation.

3.6.2.   As illustrated in Fig. 5 of Penzel, during a chained memory access (block read/write), the column address strobe signal CAS\ is pulsed [Penzel, 6:44-50]. Fig. 5 shows CAS\ as being a fixed frequency signal. Thus, Penzel discloses "receiving an external clock signal having a fixed frequency."

3.6.3.   The memory device of Penzel includes a mode register [Penzel, 3:9-11]. The mode register is a nine bit register in which two bits M_0, M_1 determine whether the read is a x1 read, a x4 read or a x8 (or x9) read [Penzel, 3:37-42]. Two further bits, M_2, M_3

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determine the number of chained accesses in a read operation (block size) [Penzel, 3:42-44 and 3:46-57]. The mode register is programmed externally via package pins P_0-P_8 [Penzel, 3:63-65]. Thus, Penzel discloses "receiving block size information, wherein the block size information defines an amount of data to be output onto an external bus in response to a read request."

3.6.4. The block read operation is described [Penzel, 4:21-26; 6:34-65]. As is clearly illustrated in Fig. 5, successive data is output in response to successive pulses of the external clock signal CAS. Thus, Penzel describes "outputting the amount of data corresponding to the block size information, in response to a read request, synchronously with respect to the external clock signal."

3.6.5. It follows that the subject-matter of claim 1 is not new.

3.6.6. As stated above, successive data is output in response to successive pulses of the external clock signal CAS. Thus, Penzel discloses that "the amount of data corresponding to the block size information is output synchronously during a plurality of clock cycles of the external clock signal."

3.6.7. It follows that the subject-matter of claim 2 is not new.

3.6.8. As shown in Fig. 5 of Penzel (understood with the necessary modifications in the case of a read operation), data is input or output in response to successive falling edges of CAS. Thus, Penzel discloses that "data is output onto the external bus synchronously with respect to a falling edge transition of the external clock signal."

3.6.9. It follows that the subject-matter of claim 9 is not new.

3.6.10. The bits M_2, M_1 of Penzel designate 1 [0,0], 2 [0,1], 4 [1,0] or 8 [1,1] accesses in a chain [Penzel, 3:47-57]. This is a logarithmic binary representation. Thus, Penzel discloses that "the block size information is a binary representation of the amount of data to be output after receipt of a read request."

3.6.11. It follows that the subject-matter of claim 10 is not new.

3.7. US Patent 4,785,428, Published November 15, 1988 ("Bajwa")

3.7.1. Fig. 1 of Bajwa is the functional block diagram of a DRAM controller (consisting of functional blocks 9, 11-13, 15-17) that controls a DRAM array 14. In the preferred embodiment, the DRAM controller itself is a chip, [Bajwa, 2:56], while the DRAM array 14 is a 1Mb conventional DRAM [Bajwa, 4:24]. The combination of the DRAM controller and the DRAM array constitutes a semiconductor memory device that interfaces with a synchronous bus 10. Thus, Bajwa discloses "a semiconductor memory device having at least one memory array which includes a plurality of memory cells" and its method of operation.

3.7.2. The DRAM controller performs the function of the bus interface of the memory device and is a clocked, self-timed device. The DRAM controller is driven by a clock having a two non-overlapping phase design [Bajwa, 2:52-54]. Four clocks PH1 and PH2 and their inverses PH1I and PH2I are disclosed as controlling the logic function (Bajwa, 2:54-59]. Fig. 4 shows how a memory access sequence is clocked with respect to PH1.

3.7.3. Bajwa further describes a clock management circuit 28 and RAS, WE, OE and CAS pin control logic which receive an external clock in the form of clock signals CLKA, CLKB, CLKC and CLKD [Bajwa, Fig. 2]. The clock management circuit in combination with the clocking signals controls timing for the memory access [Bajwa, 6:18-23]. Thus, Bajwa discloses "receiving an external clock signal having a fixed frequency."

3.7.4. The DRAM controller provides timing sequences for one to four word memory accesses [Bajwa, 8:16-19]. During a memory operation, the DRAM sequence controller 24 receives a two bit block size information code (NUMWORDS) which corresponds to the number of words for the memory access (1 to 4 words) [Bajwa, 3:63-66; Fig. 2]. A 3-bit unary encoded or 2-bit binary encoded operation code signal is supplied to a SIGNAL MUX 22 to specify whether the operation is a read, write or refresh [Bajwa, 4:6-10]. Thus, Bajwa discloses "receiving block size information, wherein the block size information defines an amount of data to be output onto an external bus in response to a read request."

3.7.5. The program RAM 20, containing the DRAM access protocols and timings, jumps to the portion of program RAM memory specifying the access protocol and timing for the number of words specified in NUMWORDS [Bajwa, 8:14-38]. The signal multiplexer 22 selects the appropriate signals from the timing sequence stored in the program RAM 20 and drives the various RAS, CAS, OE, and WE signals, along with the signals from clock management unit 28, clocking signals (CLKA-CLKD) and ARREN [Bajwa, Figs. 1 and 7]. As shown these signals are synchronous with respect to, at least, clock PH1. They are supplied to the DRAM and cause the DRAM to output the selected amount of data. The read data coming in from the DRAM is queued in the memory control unit and is output onto the external bus (AP Bus) according to a pre-programmed timing sequence which indicates the clock cycle during which the transmission of the read data may begin [Bajwa, 5:64-6:14]. The AP bus timing requires the transmission of a data word on every bus cycle [Bajwa, 6:1-2]. Thus, the data is read out synchronously with respect to the external clock signal. Accordingly, Bajwa discloses "outputting the amount of data corresponding to the block size information, in response to a read request, synchronously with respect to the external clock signal."

3.7.6. It follows that the subject-matter of claim 1 is not new.

3.7.7. The read data from the DRAM is queued in the memory control unit and is output onto the external bus (AP Bus) according to a pre-programmed timing sequence which indicates the clock cycle during which the transmission of the read data may begin [Bajwa, 5:64-6:14]. The AP bus timing requires the transmission of a data word every bus cycle [Bajwa, 6:1-2]. Thus, when more than one data word is read from the DRAM, "the amount of data corresponding to the block size information is output synchronously during a plurality of clock cycles of the external clock signal."

3.7.8. It follows that the subject-matter of claim 2 is not new.

3.7.9. The memory includes a program RAM 20 for storing "timing sequences programmed into" the DRAM controller to match the speed of any number of existing arrays [Bajwa, 2:44-45; 2:6-7]. The timing sequences are programmed into program RAM 20, which is a 53x35 array as shown in Fig. 2. Each of the 53 rows is used for programming all 35 internal transition control signals required for one clock cycle. The 53 rows are used as follows. The DRAM controller is capable of block size access of 1 to 4 words in size [Bajwa, 8:28-34], and the timing sequence for each of the 4 block size types is programmed separately, i.e. by using:

3.7.9.1. 8 rows for the timing sequence of 1-word access. [Bajwa, Fig. 6] (max delay of 8 clock cycles),

3.7.9.2. 11 rows for programming the timing sequence of a 2-word access (max delay of 11 clock cycles),

3.7.9.3. 15 rows for programming the timing sequence of a 3-word access (max delay of 15 clock cycles),

3.7.9.4.   19 rows for programming the timing sequence of a 3-word access (max delay of 19 clock cycles),

3.7.10.   This requires a total of 53 rows. Thus, program RAM 20 comprises at least four access-time registers used to specify 4 different access times corresponding to each of the 4 possible (programmable) block sizes. In this scheme, one pre-programmed signal RPYNOW signals the memory control unit to transmit the read reply packet to the AP bus [Bajwa, 5:64-6:14]. RPYNOW can correspond to any one of a number of clock cycles [Bajwa, 6:10-15]. Thus, Bajwa discloses "receiving access-time information wherein the access-time information is representative of number of cycles of the external clock signal to transpire before data is output onto the external bus after receipt of a read request." This information is programmed into a "programmable access time register."

3.7.11.   It follows that the subject-matter of claims 3-5 is not new.

3.7.12.   The block size information NUMWORDS is two bits [Bajwa, 3:63-66; Fig. 2]. These two bits correspond to block sizes of one to four words. Thus, NUMWORDS is a "binary representation of the amount of data to be output."

3.7.13.   It follows that the subject-matter of claim 10 is not new.

3.7.14.   When a read request is received, the central sequencing logic (CSL) 17 of the DRAM controller starts a timing sequence that provides all the timings required for accessing the DRAM array in each clock cycle. A SEQUENCE signal is set high to indicate that the DRAM controller is currently processing the request [Bajwa, 3:66-67; Fig. 4]. SEQUENCE is set low (inactive) when the processing of the request is completed. A RAS PRECHARGE is discussed [Bajwa, 7:15-26]. The DRAM RAS precharge time is specified by a 3-bit counter in the preferred embodiment. The counting of the precharge cycles is enabled when SEQUENCE goes inactive [Bajwa, 7:21-22]. Hence, the memory array is "automatically precharged after the read request has been executed" by the DRAM controller. When the count expires, precharge is complete and the DRAM controller is ready to process the next request (the precharge counter is also reloaded in preparation for the next read cycle) [Bajwa, 7:23-27].

3.7.15.   It follows that the subject-matter of claim 21 is not new.

3.8.   IEEE Standard for a Simple 32-Bit Backplane Bus: NuBus - ANSI/IEEE Std 1196-1987 ("NuBus")

3.8.1.   The NuBus standard is a synchronous computer backplane bus standard in which the bus is used to connect devices and to provide certain resources to the connected devices [NuBus, Fig. 1]. Conventional memory modules are one type of device that may be attached to the NuBus [NuBus, p. 42 (A.1 Note)]. Thus, NuBus discloses "a semiconductor memory device having at least one memory array which includes a plurality of memory cells" and its method of operation.

3.8.2.   The NuBus modules receive an external clock source (central system clock) [NuBus, Fig. 1; p. 4 (Section 2.1.1)]. The clock source is common to each NuBus module. The clock is a fixed frequency clock, nominally operating at 10 MHz, and is used to synchronise bus arbitration and data transfers [NuBus, p. 4 (Section 2.1.1)]. The clock signal is driven from one end of the bus to termination at the other end [NuBus, p. 44 (Section A.7)]. Thus NuBus describes "receiving an external clock signal having a fixed frequency."

3.8.3.   NuBus provides for block data transfers in block sizes of 2, 4, 8 and 16 words [NuBus, p. 11 (Section 3.1.4)]. The number of data words transferred is controlled by the master and communicated during the start cycle. The block size and block starting address is transmitted over the 32 bit multiplexed address and data lines

(which run between the master and slave devices) while the START* signal is asserted [NuBus, Fig. 4; pp. 11-13]. Thus, NuBus discloses "receiving block size information, wherein the block size information defines an amount of data to be output onto an external bus in response to a read request."

3.8.4. The slave device drives the first word of the requested data onto the 32 bit multiplexed address and data lines. The start of the data transfer is synchronous with respect to CLK* (occurring at the rising edge) [NuBus, Fig. 5; p. 12]. Blocks of data are output from the slave synchronously with respect to CLK* until the desired block size is reached [NuBus, Fig. 5]. Thus, NuBus discloses "outputting the amount of data corresponding to the block size information, in response to a read request, synchronously with respect to the external clock signal."

3.8.5. It follows that the subject-matter of claim 1 is not new.

3.8.6. As stated above, the slave device drives the subsequent words of the requested data onto the 32 bit multiplexed address and data lines. Blocks of data are output from the slave synchronously with respect to CLK* until the desired block size is reached [NuBus, Fig. 5: p. 12].: Thus, NuBus discloses that "the amount of data corresponding to the block size information is output synchronously during a plurality of clock cycles of the external clock signal."

3.8.7. It follows that the subject-matter of claim 2 is not new.

3.8.8. As discussed, blocks of data are output from the slave onto the external bus synchronously with respect to CLK* [NuBus, Fig. 5]. The data is output synchronously with respect to the rising edge: "[B]us signals shall be changed only at the rising edge of CLK*" [NuBus, Fig. 5; p. 24 (Section 3.1.8.1)]. Thus, NuBus discloses that "the data is output onto the external bus synchronously with respect to a rising edge transition of the external clock signal."

3.8.9. It follows that the subject-matter of claim 8 is not new.

3.8.10. In NuBus there are four different block sizes 2, 4, 8, and 16. There are four bits to define the block size (AD2 - AD5). If AD2 = High then the size is 2, AD3 = High then size is 4, etc. [NuBus, Table 3]. Thus, the AD lines represent the block size in binary notation. Thus, NuBus discloses that "the block size information is a binary representation of the amount of data to be output after receipt of a read request."

3.8.11. It follows that the subject-matter of claim 10 is not new.

3.9. Scalable Coherent Interface ("SCI")

3.9.1. "The Scalable Coherent Interface Project (SuperBus)", SCI-22Aug88-doc ("SCI A")

3.9.2. "Scalable Coherent Interface", SCI-28Nov88-doc10 ("SCI B")

3.9.3. P1596: "SCI A Scalable Coherent Interface", SCI-28Nov88-doc 2 ("SCI C")

3.9.4. "Proposal for Clock Distribution in SCI" - 5/5/89 ("SCI D")

3.9.5. Norsk Data Report - "A Proposal for SCI Operation" by Knut Alnes - November 1988 ("SCI E")

3.9.6. "Scalable I/O Architecture for Buses" by David V. James, SCI-28Nov88-doc3 (SCI F")

3.9.7.   SCI is an interface standard used to facilitate the assembly of nodes, or devices, including processors, I/O devices and memory [SCI A, p. 6]. A node can be a simple memory module [SCI F, Fig. "Board Architecture" p. 3]. SCI uses a 16 bit wide synchronous, packetized bus, to carry address, data and control information [SCI A, p. 4]. Thus, SCI discloses a "semiconductor memory device having at least one memory array which includes a plurality of memory cells" and its method of operation.

3.9.8.   Each SCI node receives a signal from a central system clock [SCI A, Fig. 3; SCI B, p. 2]. Thus, SCI discloses "receiving an external clock signal having a fixed frequency."

3.9.9.   An SCI node receives a request packet with target, source, control and address information [SCI A, Figs. 4 and 15]. SCI supports operations of 32, 64, 128 and 256 data blocks, and 1-16 byte subsets of the 16-byte block [SCI A, p. 8; Fig. 11; SCI C, p. 11]. The block size information is conveyed in the transfer code, which forms part of the control information received by the node [SCI A, Figs. 14 and 15; p. 14; SCI C, p. 13 (Header Command)]. Thus, SCI discloses "receiving block size information, wherein the block size information defines an amount of data to be output onto an external bus in response to a read request."

3.9.10. The targeted device outputs a variable size data block (i.e., Data Word 0 to Data Word n) in accordance with the block size information [SCI A, Fig. 15; p. 14]. All inputs and outputs on the bus are synchronous with respect to the external system clock [SCI A, p. 3]. All nodes in SCI operate synchronously with respect to the system clock. Thus, SCI discloses "outputting the amount of data corresponding to the block size information, in response to a read request, synchronously with respect to the external clock signal."

3.9.11. It follows that the subject-matter of claim 1 is not new.

3.9.12. The variable size data block (i.e., Data Word 0 though Data Word n) is output in accordance with the block size information [SCI A, Fig. 15; p. 14]. Successive data words are output during a plurality of clock cycles. All inputs and outputs on the bus are synchronous [SCI A, p. 3]. All nodes in the SCI operate synchronously with respect to the system clock. Thus, SCI discloses that "the amount of data corresponding to the block size information is output synchronously during a plurality of clock cycles of the external clock signal."

3.9.13. It follows that the subject-matter of claim 2 is not new.

3.9.14. SCI discloses the use of both clock edges for changing data [SCI B, p. 2; SCI D, p. 2]. Thus, SCI discloses that "the data is output onto the external bus synchronously with respect to a rising edge transition of the external clock signal" and that "the data is output onto the external bus synchronously with respect to a falling edge transition of the external clock signal."

3.9.15. It follows that the subject-matter of claims 8 and 9 is not new.

3.9.16. The "read request" and "block size information" are both contained within a "request packet" [SCI A, pp. 4 and 14; Figs. 9 and 15].

3.9.17. It follows that the subject-matter of claim 12 is not new.

3.9.18. SCI discloses the use of an internal clock signal generated by a digital phase lock loop to eliminate clock skew [SCI B, p. 2; SCI D, pp. 1-5]. The internal clock is used for outputting data on the external bus [SCI B, p. 2]. Thus, SCI discloses "generating a first internal clock signal using the external clock signal wherein the amount of data corresponding to the block size information is output on to the external bus synchronously with respect to the first internal clock signal."

3.9.19. It follows that the subject-matter of claim 13 is not new.

3.9.20. As discussed, SCI discloses the use of a digital phase lock loop to generate an internal clock signal [SCI B, p. 2; SCI D, pp. 1-5]. The digital PLL disclosed in the reference D is a DLL: it shows the use of a delay line and no VCO. Thus, "the first internal clock signal is generated by a delay locked loop."

3.9.21. It follows that the subject-matter of claim 14 is not new.

3.9.22. Each SCI node has a unique 16 bit identification code stored in a register [SCI A, p. 6; SCI E, pp. 1-4].). Thus, SCI discloses that "the semiconductor memory further includes a programmable identification register to store an identification value to identify the memory device from a plurality of other memory devices on the external bus." The ID information is sent in the request packet and received by the SCI nodes [SCI A, pp. 6-7; Fig. 9]. Thus, SCI discloses "receiving identification information."

3.9.23. SCI nodes determine whether the target identification code in the request packet matches the identification code of the node [SCI E, pp. 1 and 5-6]. The targeted node outputs a variable size data block (i.e., Data Word 0 though Data Word n) in accordance with the block size information [SCI A, Fig. 15; p. 14]. All inputs and outputs on the bus are synchronous with respect to the external system clock [SCI A, p. 3]. All nodes in the SCI operate synchronously with respect to the system clock. Thus, SCI discloses "determining whether the identification information corresponds to the identification value stored in the programmable identification register wherein, when the identification information corresponds to the identification value, the amount of data corresponding to the block size information is output onto the external bus synchronously with respect to the external clock signal."

3.9.24. It follows that the subject-matter of claim 17 is not new.

3.9.25. The identification register contains a Global ID and Local ID. The Global ID is the 10 MSB of the node ID and is used to identify a ring on the SCI network (which contains several nodes) [SCI E, p. 1] Thus, SCI discloses that "the programmable identification register stores an identification value to identify the memory device and a plurality of other memory devices on the external bus."

3.9.26. It follows that the subject-matter of claim 18 is not new.

3.9.27. Node ID's are assigned during an initialisation sequence after reset of the SCI. A hardware or software based protocol is employed to assign node identifications. Following the assignment of node identification, the SCI master will initialise the interface registers of the various nodes and will cause the node ID to be written into the individual registers [SCI E, pp. 2-4]. Thus, SCI discloses that "the programmable identification register is programmed after power is applied to the memory device during initialisation of the memory device" and that "the programmable identification register stores an identification value during an initialisation sequence of the memory device."

3.9.28. It follows that the subject-matter of claims 19 and 20 is not new.

3.10. US Patent 4,785,394, Published November 15, 1988 ("Fischer")

3.10.1. Fischer describes a multiprocessor computer system arranged around a split-transaction bus [Fischer, abstract]. Bus devices are notionally classified into "initiators," including CPU modules, and "responders," including memory modules [Fischer, Fig. 1]. The split-transaction bus carries all information between bus devices and no point-to-point signals are used [Fischer, 7:36-40]. Each of the memory modules includes conventional memory components [Fischer, 6:6-7]. Some

or all of the memories in the modules may be cache memories [Fischer, 6:17-19].
Both the conventional memories and cache memories are semiconductor memories.
Each includes semiconductor logic components [Fischer, 5:47-49]. Thus, Fischer
discloses a "semiconductor memory device having at least one memory array
which includes a plurality of memory cells."

3.10.2. A typical responder module is illustrated in Fig. 2 (right hand side) of Fischer. As
can be seen, it includes clock receivers 76 that receive clock signals B.CLK 0,
B.CLK 1. As shown in Figs. 3A and 3B of Fischer, these clock signals are fixed
frequency square waves in quadrature [Fischer, 8:53-55]. They are generated by a
backplane clock generation circuit 74. Clock skew is eliminated by the use of equal
length clock signal conductors, ensuring reliable synchronisation [Fischer, 8:33-50].
Thus, Fischer discloses "receiving an external clock signal having a fixed
frequency."

3.10.3. The initiating transaction of a read operation is illustrated in Fig. 6B [Fischer, 10:32-
35]. The format of the address information transmitted in bus cycle X of Fig. 6B is
shown in Fig. 7A [Fischer, 14:26-29]. It includes three fields. A first field 86 is a
two-bit field indicating the nature of the transaction (read, test and set, scrub or
write) [Fischer, 13:59-64]. A second field 88 is a 28 bit memory address that
identifies the responder to which the request is addressed and the address within that
responder [Fischer, 13:64-14:4]. A third field 90 indicates whether one, two or four
doublewords are to be transferred in response to the request [Fischer, 14:4-8]. Thus,
Fischer discloses "receiving block size information, wherein the block size
information defines an amount of data to be output onto an external bus in
response to a read request."

3.10.4. Each clock receiver 76, illustrated in Fig. 4 of Fischer, generates four internal clock
signals B0 ... B3, one quarter cycle out of phase with each other [Fischer, 9:6-25;
Figs. 3C-3F]. The format of data placed on the bus in response to a read request is
illustrated in Fig. 7B. As shown in Fig. 6B, one doubleword is output per bus cycle.
The Fischer system is synchronous [Fischer, 8:33-50; 9:26-38]. Control, address and
data signals transferred from bus master to bus slave (initiator to responder or vice
versa) are designated as signals B.DAT31-0 [Fischer, 15:43-50]. These signals are
asserted on the rising edge of B0 and negated on the rising edge of B3 (three
quarter-cycles later). B0 is synchronised with external clock signal B.CLK 1
[Fischer, Figs. 3A, 3C and 4]. Thus, Fischer discloses "outputting the amount of
data corresponding to the block size information, in response to a read request,
synchronously with respect to the external clock signal."

3.10.5. It follows that the subject-matter of claim 1 is not new.

3.10.6. As discussed above and as shown in Fig. 6B, one doubleword is output per bus
cycle. The Fischer system is synchronous [Fischer, 8:33-50; 9:26-38]. Control,
address and data signals transferred from bus master to bus slave (initiator to
responder or vice versa) are designated as signals B.DAT31-0 [Fischer, 15:43-50].
These signals are asserted on the rising edge of B0 and negated on the rising edge of
B3 (three quarter-cycles later). B0 is synchronised with external clock signal B.CLK
1 [Fischer, Figs. 3A, 3C and 4]. Thus, Fischer discloses that "the amount of data
corresponding to the block size information is output synchronously during a
plurality of clock cycles of the external clock signal."

3.10.7. It follows that the subject-matter of claim 2 is not new.

3.10.8. Again, as discussed above, control, address and data signals B.DAT31-0 are asserted
on the rising edge of B0, which is synchronized with external clock signal B.CLK 1
[Fischer, Figs. 3A, 3C and 4]. Thus, Fischer discloses that "data is output onto the
external bus synchronously with respect to a rising edge transition of the
external clock signal."

3.10.9.   It follows that the subject-matter of claim 8 is not new.

3.10.10. No inventive step would be involved in advancing or retarding all of the clock
          signals of Fischer by one half clock cycle. Thus, bus cycles would begin and end on
          the rising edge of B2 rather than B0. In that case, "data is output onto the external
          bus synchronously with respect to a falling edge transition of the external clock
          signal."

3.10.11. It follows that the subject-matter of claim 9 is obvious.

3.10.12. As discussed above, the third field 90 of the address information transmitted in bus
          cycle X of Fig. 6B indicates whether one [0,0], two [0,1] or four [1,1] doublewords
          are to be transferred in response to the request [Fischer, 14:4-8]. Thus, the two bits
          are a logarithmic binary representation of the block size in units of 32 bits
          (doublewords). Therefore, Fischer discloses that "the block size information is a
          binary representation of the amount of data to be output after receipt of a read
          request."

3.10.13. It follows that the subject-matter of claim 10 is not new.

3.10.14. As discussed above, a two-bit field 90 of the address information transmitted in bus
          cycle X of Fig. 6B contains the encoded block size information. Thus, Fischer
          discloses that "the read request and block size information are included in one
          request packet."

3.10.15. It follows that the subject-matter of claim 12 is not new.

3.10.16. As discussed above, control, address and data signals B.DAT31-0 are asserted on
          the rising edge of internal clock signal B0. Thus, Fischer discloses "generating a
          first internal clock signal using the external clock signal wherein the amount of
          data corresponding to the block size information is output on to the external
          bus synchronously with respect to the first internal clock signal."

3.10.17. It follows that the subject-matter of claim 13 is not new.

3.10.18. As discussed above, the control, address and data signals B.DAT31-0 are asserted on
          the rising edge of internal clock signal B3. Thus, Fischer discloses "generating first
          and second internal clock signals using the external clock signal wherein the
          amount of data corresponding to the block size information is output on to the
          external bus synchronously with respect to the first and second internal clock
          signals."

3.10.19. It follows that the subject-matter of claim 15 is not new.

3.10.20. As discussed above, the format of the address information transmitted in bus cycle
          X of Fig. 6B is shown in Fig. 7A [Fischer, 14:26-29]. It includes three fields. The
          second field 88 is a 28 bit memory address that identifies the responder to which the
          request is addressed and the address within that responder [Fischer, 13:64-14:4].
          Thus, Fischer discloses "receiving identification information." No point to point
          signals are used [Fischer, 7:36-40]. Thus, each memory module must decode the
          MSBs of the address to determine whether to respond. Accordingly, the module
          must contain an internal address space identification with which to compare the
          MSBs. That address space identification must be programmable, and in Fischer it is
          received from the backplane [Fischer, 16:21-27]. Thus, Fischer discloses "a
          programmable identification register to store an identification value to identify
          the memory device from a plurality of other memory devices on the external
          bus" and "determining whether the identification information corresponds to
          the identification value stored in the programmable identification register
          wherein, when the identification information corresponds to the identification

value, the amount of data corresponding to the block size information is output onto the external bus synchronously with respect to the external clock signal."

3.10.21. It follows that the subject-matter of claim 17 is not new.

3.10.22. As discussed above, Fischer describes receiving an address space identification from the backplane. This must be done during an initialisation sequence following power-up or the memory would be unable to respond to requests.

3.10.23. It follows that the subject-matter of claims 19 and 20 is not new.

4. **LACK OF INVENTIVE STEP ART. 56 EPC**

4.1. The matter disclosed in the Parent Application does not support any claim purporting to cover buses other than the highly multiplexed bus described or read requests other than read request packets. In proceedings brought in the UK, France and Germany under the patent arising from the Parent Application, the patentee has asserted that the terms "external bus" and "request" in granted claim 1 of that patent should be afforded an interpretation wider than that supported by the Parent Application. The following discussion assumes that such a wider interpretation may be advanced by the patentee in respect of the Patent.

4.2. The subject-matter of claims 1-21 of the Patent is obvious even if entitled to the declared priority date of April 18, 1990.

4.3. Other Relevant Documents

4.3.1. Programmable Block Size Reads (Claims 1, 2, 8-10 and 12)

4.3.1.1. Japanese Patent Application No. S63-142445, Published June 14, 1988, and English Translation ("Taguchi")

4.3.1.1.1. Taguchi discloses a memory device having an array formed from a plurality of memory cells [Taguchi, Fig. 1 in conjunction with Figs. 5 and 6 and 4:27-29] and its method of operation.

4.3.1.1.2. A data length register holds the entire size of the data to be accessed [Taguchi, p. 4]. In addition, Taguchi discloses the use of a block length register to define the size of each block and a data length register to define the number of blocks that are to be accessed in an operation [Taguchi, p. 4]. Block data of the size specified in the block length register is read from the memory, the next block of memory to be accessed is calculated from the starting address plus the block size, another block read is performed, and the new starting address is calculated [Taguchi, p. 4]. Counters monitor the number of block reads left in the block access operation. The reading process continues until the amount of data specified in the data length register is output [Taguchi, p. 4]

4.3.1.2. US Patent 4,315,308, Published February 9, 1982 ("Jackson")

4.3.1.2.1. Jackson discloses a system with a microprocessor attached to a Bus Interface Unit (BIU) which provides for interface control of data transfers between the processor and devices, including memory devices [Jackson, 4:17-21]. Each unit in the system receives a clocking signal CLKA to control synchronisation [Jackson 4:36-44; 5:36-38]. CLKA is of fixed frequency [Jackson, Fig. 2].

4.3.1.2.2. Jackson discloses block modes of up to 20 bytes per read request [Jackson, 3:16-19; 6:4-6]. Specifically, Jackson supports transactions of 1, 2, 4, 6, 8, 10, 16 and 20 bytes [Jackson, Fig. 3]. A three bit long

sequence in a control specification is used to specify block size
[Jackson, Fig. 3 (bits 10, 11 and 12); 3:29-30]. The memory returns the
requested number of data bytes to the BIU [Jackson, 6:8-12]. As the
memory continues to output the data, the BIU buffers and aligns the
data and then transfers the data across the ACD bus to the processor.
This process is repeated until the processor has received the requested
number of bytes [Jackson, 6:20-23]. A read operation takes place over a
plurality of clock cycles [Jackson, 5:38-39; Fig. 9]. The block size
information is a binary representation of the amount of data to be output
[Jackson, Fig. 3].

4.3.1.2.3.   Jackson discloses the use of a control specification whereby the
operation code (read request), block size information and the eight least
significant bits of the address are placed on the bus at the same time
[Jackson, Figs. 2 and 3; 5:53-58].

4.3.2.   Programmable Access Time Register (Claims 3-7 and 11)

4.3.2.1.   Japanese Patent Application Sho 62-71428, Published October 5, 1988,
and English Translation ("Yamaguchi")

4.3.2.1.1.   Yamaguchi describes a dual-port RAM that has both random access I/O
and serial access I/O capabilities [Yamaguchi, 3:1-3; 7:3-9]. The
random access and serial ports IO1 ... IO3, SIO1 ... SIO 3 and address
lines A0 ... Ai are provided to allow the device to connect to an
external bus. The RAM includes four memory arrays M-ARY1 ... M-
ARY4 [Yamaguchi, 8:10-12]. Each memory cell array M-ARY1 ... M-
ARY4 comprises $m+1$ word lines and $n+1$ sets of complementary data
lines which intersect at $(m+1) \times (n+1)$ memory cells [Yamaguchi, 8:17-
20]. The device may be formed on a single chip [Yamaguchi, 7:4-6].

4.3.2.1.2.   The dual-port RAM includes a timing control circuit TC that receives a
number of external control signals [Yamaguchi, 18:10-13; Fig. 1]. One
such external control signal is an external serial clock signal SC that is
generated off-chip [Yamaguchi, 18:13-16]. The external serial clock
signal SC is used to ensure stable synchronisation of the serial output
operation of the dual-port RAM with the dot rate of a high-resolution,
high-dot-rate external CRT [Yamaguchi, 28:7-15]. The external serial
clock signal is therefore a signal of a fixed frequency linked to the dot
rate of the external CRT.

4.3.2.1.3.   The timing control circuit includes a counter circuit CTR [Yamaguchi,
19:12-15]. A counter is a register that is capable of incrementing or
decrementing the value it contains. Many microprocessor internal
registers, including program counter (PC) and accumulator (AC)
registers are also counters of this kind. An alternative arrangement is
discussed in which a register latches the count value and a count-up
counter is used to count from zero until its output matches the value in
the register [Yamaguchi, 28:19-29:1]. In the preferred embodiment, the
counter of Yamaguchi is loaded with a value presented on the parallel
I/O lines IO1 ... IO4 on the falling edge of the row address strobe
signal RAS\ [Yamaguchi, 21:12-17; 25:8-11]. Once loaded with this
value, the counter circuit counts down to zero in synchronism with an
internal clock signal, the counter advancing timing signal ϕcp
[Yamaguchi, 21:18-22:3]. This internal clock signal ϕcp is generated by
the timing control circuit TC from, and has the same frequency as, the
external serial clock signal SC. It is merely a slightly delayed version of
the external serial clock signal SC owing to the gate delays of inverters
N1 and N2 and the AND gate AG2 of the timing control circuit TC
[Yamaguchi, 23:8-14, Figs. 1 & 3]. The overall result is that the counter

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circuit CTR counts clock cycles of the external serial clock signal SC
[Yamaguchi, 19:12-15].

4.3.2.1.4.   As will be described below, the counter circuit is used to delay the
             output of serial data by a number of clock cycles corresponding to the
             value loaded into the counter circuit CTR [Yamaguchi, 27:19-21].

4.3.2.1.5.   In accordance with a further internal clock signal φc, the serial I/O
             circuit latches the data presented by data registers DR1 ... DR4 on
             complementary data lines CDS1 ... CDS4 to the serial data lines SIO1
             ... SIO4 and hence to an external bus [Yamaguchi, 19:17-19]. Clock
             signal φc is synchronised to external serial clock signal SC [Yamaguchi,
             26:17-19]. After the first transition of the internal clock signal φc, it is
             also used to shift a shift register of a pointer PNT that points to the
             current position in the data registers DR1 ... DR4, thus accessing the
             next data in the data registers DR1 ... DR4 [Yamaguchi, 26:19-27:7].
             Data is output in accurate synchrony with the external serial clock
             signal SC only once an internal strobe signal φci, generated when the
             counter CTR reaches to zero, has been asserted.

4.3.2.1.6.   The serial I/O circuit drives data presented on the complementary data
             lines CDS1 ... CDS4 to the serial data lines SIO1 ... SIO4 in
             accordance with the internal clock signal φc. One or other edge must be
             used to control STO. Fig. 3 shows that the output data transitions on the
             rising edge of φc and on the rising edge of the serial clock signal SC.

4.3.2.1.7.   As explained above, the number of clock cycle delays introduced into a
             serial read operation by the counter circuit CTR is equal to the value
             stored in it during the read request. That value can be between 0 and 15.
             The value stored is therefore representative of one of a plurality of
             different delay times.

4.3.2.2   GigaBit Logic, 1989 GaAs IC Data Book & Designer's Guide, August
             1989, 12G014 256x4-Bit Registered Self-Timed SRAM ("GigaBit")

4.3.2.2.1.   Gigabit describes a 256x4-bit static RAM fabricated using Gallium
             Arsenide (GaAs) technology ("The 12G014"). The 12G014 is a self-
             timed SRAM ("STRAM"), running at a fixed frequency of 400 MHz.
             The clock cycle is therefore 2.5 ns. The 12G014 STRAM has
             differential clock inputs CLK and CLK\, as shown in the block diagram
             on page 2-3. The differential clock inputs connect to an output clock
             generator functional block, which must include clock receiver circuitry
             to receive the differential clock inputs.

4.3.2.2.2.   The 12G014 is a x4 memory, with four output drivers (Q0-Q3)
             outputting data onto the bus in response to a read request. The output is
             fully registered (double latch) as shown in the block diagram on page 2-
             3. The output register is clocked synchronously to the external clock via
             the agency of the output clock generator that generates an internal clock
             from the complementary clock inputs CLK and CLK\. Hence, the
             output operation is done synchronously with respect to the external
             clock.

4.3.2.2.3.   The 12G014 has three output modes, namely latch mode, register mode
             and transparent mode. The transparent mode is asynchronous (similar to
             conventional SRAMs). Both the latched mode and register mode are
             clocked. In register mode, memory access takes place during the clock
             cycle in which the read request is received. Valid output data is
             presented to the on-chip output drivers. At the next rising edge of the

clock signal, i.e. a full 25 ns clock cycle after the read request is received, this data is loaded into the output drivers and propagates to the data output pins, and hence the bus, where it is held for a full cycle. This is shown and described in the timing diagram on page 2-6.

4.3.2.2.4.   In latch-mode, memory access again takes place during the clock cycle in which the read request is received. Valid output data is presented to the on-chip output drivers. However, these output drivers are driven transparent at the falling edge of the clock signal to allow valid data to appear on the data output pins, and hence on the bus, as soon as possible. The duty cycle of the clock is changed so that the falling edge arrives after less than one half clock cycle. The output drivers are driven transparent at this falling edge and latched at the next rising edge to hold data over to the falling edge of the next clock cycle. This is shown and described in the timing diagram on page 2-7.

4.3.2.2.5.   The output mode is programmed by applying one of three signal levels to a MODE pin, as described on page 2-4: Vss level gives register mode, Vdd gives latch mode and Vcc gives transparent mode. The mode pin signal is received in the output clock generator where it must be decoded. The circuitry that decodes the mode pin signal and produces the decoded logical outputs is programmable until the mode pin is connected and thereafter outputs the value programmed into it. The value programmed into this register determines the output mode and, in particular, the output delay.

4.3.2.2.6.   As discussed above, in register mode, data output takes place on the rising edge of the internal clock, which is synchronised with the external clock signal CLK. The Fig. on page 2-3 includes an "Output Clock Generator," which generates internal clock signals from CLK and CLK'. These internal clock signals drive the output register. In register mode, data is driven onto the bus at the rising edge of the internal clock signal.

4.3.2.2.7.   As discussed above, the value programmed into the access-time register determines the output mode and, in particular, the output delay. It is representative of one of a plurality of different delay times.

4.3.2.3.   US Patent No. 4,499,536, Issued February 12, 1985 ("Gemma")

4.3.2.3.1.   Gemma describes a processor-based SCU that interfaces with a main memory including a plurality of memory cells arranged as one or more memory arrays [Gemma, 3:65]. The memory arrays may be in a number of configurations [Gemma, 6:25-32]. The SCU includes a controller 17 that receives a clock signal T₂ synchronised with the processor machine cycle [Gemma, 4:26-35; Fig. 2]. This is received by AND gates 29 and 24 within the controller 17. Timing control signals that drive a counter 25 are generated from the clock signal T₂ [Gemma, Fig. 2].

4.3.2.3.2.   The SCU 17 receives memory related instructions from a current instruction register via a signal line 101 under the control of an execution unit. Control information is sent to the SCU from the execution unit via a signal line 102. The control information determines the "type of main memory access, that is, read (FE), full write (ST) and partial write (PST)" [Gemma, 3:10-17]. The generation of a main memory access start signal (EX) that is sent to the main memory is described. The signal has a pulse width predetermined by the timing of timing signals T₀ and T₁ [Gemma, 3:18-41]. Subsequently, the SCU 19 sends a GFDR signal to the main memory on signal line 19 to instruct the main memory to send readout data to a data bus 118 and sends an

ADV signal to the processor on signal line 120 to instruct a read data register in the processor to read the data on the data bus 118 [Gemma, 3:52-56]. The content of the read data register is sent to the execution unit 2 via a data bus 122 [Gemma, 3:58-60]. It is implicit in the requirement for the main memory to respond to the GFDR signal that the main memory includes output drivers that respond to the signal. These output drivers output data onto the data bus 118.

4.3.2.3.3.   The SCU includes a controller 13, which is shown in detail in Fig. 2. The controller 13 has "configuration registers 20 and 21 which retain identification flags for the machine cycle of the processor and identification flags concerning the access time of the main memory cells, respectively" [Gemma, 3:61-65]. As described, the controller includes "a counter 25 for counting an elapsed time after the signal EX of a predetermined pulse width has been produced, a decoder 26 for decoding the count of the counter 25, a control circuit 27 for producing the signals GFDR and ADV ... based on the output of the decoder 26" [Gemma, 4:4-10]. Therefore, the timing of the GFDR and ADV signals is determined with reference to the start of the count of the counter. The count is begun with reference to the EX signal that has a predetermined pulse width [Gemma, 3:39-41]. The counter counts according to the clock signal T_2 synchronized with the machine cycles [Gemma, 4:26-35].

4.3.2.3.4.   The configuration registers 20 and 21 of the controller 13 are initialised to contain one of three machine cycle identification flags and one of three main memory identification flags [Gemma, 4:11-17]. The output from the configuration registers 20 and 21 are supplied to the control circuit 22 via signal lines 200 and 201 [Gemma, 4:22-25]. The counter 25 is reset in response to the memory signal EX being low [Gemma, 4:32-35]. The output of the counter, representing a number in binary form, 20-23, is fed to a decoder 26 [Gemma, 4:35-38].

4.3.2.3.5.   According to Gemma, "the relation between the combinations of the identification flags m_k (k=1~3) and the n_j (j=1~3) and the send timings of the signals GFDR, ADV and PSYC. The send timings are represented by the counts C_1~C_{12} of the number of machine cycle counted after the signal EX has been produced. These counts are predetermined based on the response performance of the processor and the main memory, i.e. based on the contents of the configuration registers [Gemma, 4:53-60]. The following example of the timing is given: "when the identification flags m_1 and n_1 are set to "1", respectively, the signal GFDR is sent at the timing C_i and the signal ADV is sent at the timing C_{i+1}" [Gemma, 4:60-63]. Thus, once the EX signal has been produced, that is, once the memory has been instructed to execute a read, the signal GFDR is sent to the memory to instruct it to output the result of the read at a time of C_i which is measured in terms of machine cycles of the processor, the number being determined by the contents of the configuration registers. Having issued the signal GFDR, the controller then issues the signal ADV at a time of C_{i+1} to instruct the read data register to read the output from the memory.

4.3.2.3.6.   As discussed above, the timing signal T_2 is synchronous with the machine cycles. When signal EX goes high, AND gate 24 detects the rising edge of signal T_2. Thus, counter 25, and decoder 26 change state on the rising edge of T_2. C_1 transitions from low to high [Gemma, 4:41-44]. The same will happen with C_{i+1}~C_{i+2}. Data selecting circuits 22 select, according to the input s0~s4, one of the signals C_1~C_m applied to input terminals d0~d4. The data selecting circuits reproduce the selected signal at a corresponding output terminal [Gemma, 5:48-53].

Unless the data selecting circuits are enabled, the outputs are zero [Gemma 5:60-62].

4.3.2.3.7.   Thus, the output "u" of a data selecting circuit reflects the state of a corresponding selected input, $C_{i+1}-C_{i+4}$. Since the signals $C_{i+1}-C_{i+4}$ are positive going and the disabled output of the selecting circuits is zero, the outputs "u" are also positive going in response to a rising edge of T_1, which is in turn synchronised to an external clock. The signal GFDR, which controls the output of the data from the read data register, is derived from the second data selecting circuit 66.

4.3.2.3.8.   The initialisation of the configuration registers 20 and 21 is described as follows. In the initialisation of the processor, one of the identification flags m_1-m_n and one of the identification flags t_1-t_n, are set to "1". The operation may be carried out by a known technique, such as by loading a microprogram into the control memory during the initialisation of the processor [Gemma, 4:9-22].

4.3.2.3.9.   The values, m_1-m_n and t_1-t_n, stored in the configuration control registers clearly control the timing of the output signals. The value stored in the programmable access time register is representative of one of a plurality of different delay times.

4.3.2.4.   Japanese Patent Application Sho 62-185253, Published January 31, 1989, and English Translation ("Kumagai")

4.3.2.4.1.   Kumagai discloses a main storage unit MS 4 that includes RAM memory arrays RAM0, RAM1, RAM2, RAM3 [Kumagai, Fig. 1]. The memory device MS 4 is clocked by an external clock source 5. That clock source is at least common to the memory device MS 4 and the memory controller SCU. It is a fixed frequency clock [Kumagai, Fig. 4]. The clock is used to clock all the interfaces of MS 4 which are all latched: command/address buffer MRQ 20, input data MSD 21 and output data MFD 30 [Kumagai, 4:8-22]. The circuitry to receive the external clock is not specified in Kumagai, but it must exists and can simply be an input buffer.

4.3.2.4.2.   The control unit of memory device MS 4, MCR 51, contains the clock counter circuitry shown in Fig. 3. The circuitry includes latches C0 ... C3. These latches store a value representative of a number of clock cycles of the external clock, which is input to the circuitry at 316 (clock T0). The combination of blocks 300, 301, 318 and 319 of Fig. 3 is a clock counter that would signal (see input to block 102) when the clock count reaches the delay value stored in latches C0-C3. That signal then is used to trigger CAS\ (through the clock phase selection circuitry 102, 303, 304 and 305). Hence, data in RAM0-3 is accessed only after the number of clock cycles stored in C0-C3 has transpired. The data is then sent to the memory output latch MFD 30 to be output at a clock edge to the requesting device SCU 3 [Kumagai, 5:10-27]. Latches C0-C3 are programmable in the sense that they hold whatever values were read into them. Because C0-C3 are part of MCR 51, which is programmed by SCU 3 via MRQ 20, C0-C3 are programmable by the SCU 3 via that interface.

4.3.2.4.3.   Each of the synchronous interfaces to the memory device MS 4 of Kumagai, namely the command/address interface at MRQ 20, the input data interface at MSD 21 and the output data interface MFD-30 can each be one or many bits wide. That output operation is in response to a read request from SCU 3 via command interface MRQ 20 [Kumagai, 4:32-5:2]. The output operation is delayed until after a specified number

of clock cycles has transpired. The output operation is synchronous with respect to the external clock because MFD 30 is a latch.

4.3.2.4.4.   As shown in Fig. 3 and 4 of Kumagai, the memory device MS 4 can be programmed to output data at any one of four phases of the external clock. The phase number value is stored in latches T0-T3 (310-313). One of those four values (e.g. 3 out of a 0-3 range) corresponds to a synchronous output that is synchronised with respect to a rising edge of the external clock signal.

4.3.2.4.5.   The value for access time in Kumagai is stored in latches C0-C3. Latches are devices that hold values clocked in after power is applied. The latches C0-C3 are programmed via the command interface MRQ 20. In most cases, it would be done once and for all after power up, because in a given system the memory access time and processor machine cycle will not change. This amounts to programming during an initialisation sequence of the memory device following power up. The latches C0-C3 of Kumagai allow four different access times to be programmed into the memory device MS 4 [Kumagai, 5:27, Fig. 3: blocks 300, 318, 319 and 514].

4.3.3.   Delay Locked Loop (claims 14 and 16)

4.3.3.1.   At the priority date of the Patent, DLLs were common general knowledge. DLLs enable regularly cyclic digital signals at the same frequency to be synchronised with one another.

4.3.3.2.   UK Patent Application GB-2,197,553, Published May 18, 1988 ("Lofgren")

4.3.3.2.1.   Lofgren describes a digital phase locked loop circuit (DLL) [Lofgren, abstract]. One principal application of the DLL described is to provide "optimum timing for control of high speed dynamic RAM devices" [Lofgren, 1:14-18]. Lofgren discloses the use of two identical delay lines. One delay line 12 is clocked by a local oscillator 20 and used to calibrate the DLL. The other delay line 18 is used to provide an accurate delay to an input signal [Lofgren, 1:130-2:5].

4.3.3.2.2.   Each delay line 12, 18 consists of plural delay elements D_n, the amount of delay introduced by each of which being controlled by the level of two control signals VCP, VCN, generated by a charge pump 16 in response to phase errors detected in the first delay line 12 [Lofgren, 3:78-114; 4:23-33; 4:62-68; 5:78-96]. The delay introduced by the first delay line 12 is varied until it is exactly one period of the local oscillator 20 [Lofgren, 4:104-106]. Identical control signals are then applied to the second delay line 18. It is then known that each of the n delay elements D_n in the second delay line 18 will introduce a delay of one n^o of the period of the local oscillator. The second delay line is a multi-tap line, allowing one of a plurality of delays to be selected [Lofgren, 2:5-13].

4.3.3.3.   IEEE Journal of Solid State Circuits, Vol. 25, No. 1, February 1990, "An On-Chip Smart Memory for a Data-Flow CPU" ("Uvieghara"), as Exemplifying Common General Knowledge

4.3.3.3.1.   Uvieghara describes a high performance substrate CPU that has an embedded smart memory of the type known as a "register alias table" ("RAT"). The RAT is a multi-port content-addressable memory supporting branch prediction and exception handling. An experimental 1240 bit RAT is described [Uvieghara, abstract]. The RAT is a

synchronous DRAM [Uvieghara, Fig. 5] having a block read mode [Uvieghara, 87:2-4].

4.3.3.3.   The RAT uses a PLL-based clock generator on-chip [Uvieghara, Fig. 13; and p. 92 "All clocks are generated by a ... PLL-based clock generator."]

4.3.3.4.   US Patent No. 4,637,018, Issued January 13, 1987, ("Flora"), as Exemplifying Common General Knowledge

4.3.3.4.1.   Flora discloses a DLL that is designed to synchronise the outputs of a distributed clock driver circuit with an accurately delayed external clock signal [Flora, 3:6-16]. As the device is a clock distribution system, exact synchronisation with the external clock signal is not essential, but synchronisation of the outputs of several chips with each other is [Flora, 3:22-28]. For this reason the external clock signal receiving line is bifurcated. One branch is subject to an accurate delay and the other includes a multi-tap delay line introducing a variable delay to the clock driver circuit. The outputs of the clock driver circuitry are synchronised to the delayed external clock [Flora, 3:60-68]. However, if accurate phase synchronisation with the external clock were required, the delay line would be removed, or re-introduced in the same branch as the variable delay to give an accurate delay of just short of one clock cycle. In this way, the outputs of the clock driver circuitry would be accurately synchronised to the external clock. This all results from the application of common general knowledge at the priority date.

4.3.3.5.   Japanese Patent Application JP-A-01-284132, published November 15, 1989, and English Translation ("Kosugi"), as Exemplifying Common General Knowledge

4.3.3.5.1.   Kosugi discloses a digital phase locked loop (DPLL) that is used for synchronising the internal read clock 3 (clocking the output) of a memory device 1 to its internal write clock 2 (clocking the input). The memory write clock 2 is itself generated from an external clock.

4.3.3.6.   Motorola MC88200 Cache/Memory Management Unit User's Manual, Published 1988, as Exemplifying Common General Knowledge ("MC88200")

4.3.3.6.1.   The MC88200 is a single chip synchronous device that contains high-speed cache memory. The MC88200 has a large number of on-chip, dynamically programmable configuration registers, as shown in table 1-1. The device generates on-chip all internal timing signals from an external clock signal CLK. The MC88200 internal clock is normally phase locked to the external clock signal CLK in order to minimise the skew between the external and internal signals [MC88200, page 4-9].

4.3.3.7.   It was obviously desirable on the priority date of the Patent that internal device clock signals should be synchronised as closely as possible with the external clock signal.

4.3.3.8.   The objective problem to be solved by a device according to granted claims 14 or 16 is the provision of more accurately synchronised internal clock signals. This problem is solved by using a DLL, as would have been well known to a person skilled in the art at the priority date.

4.3.3.9.   It follows that the subject-matter of claims 14 and 16 is obvious.

4.3.4.   Dual Internal Clocks (Claim 15)

4.3.4.1.   US Patent 4,680,738, Published July 14, 1987 ("Tam")

4.3.4.1.1.   Tam discloses a memory device that can operate in a conventional access mode and a high speed sequential (block) mode [Tam, abstract]. To facilitate the high speed sequential mode, the memory is organised into two arrays [Tam, Fig. 1]. A separate internal clock is derived for each array (CKL; CKR) from an external clock signal CK. The two internal clocks are 180° out of phase with one another (Tam, Fig. 2; 3:63-4:5 *et seq*].

4.3.4.2.   US Patent 4,330,852, Published May 18, 1982 ("Redwine")

4.3.4.2.1.   Redwine discloses a serial input/output memory device in which the input/output is performed in units of 256 bits [Redwine, abstract; Fig. 1]. To increase the serial access speed, the memory is organised into two arrays [Redwine, 2:55-60; Fig. 1]. A separate internal clock is derived for each array (Φ1; Φ2) from an external clock signal Φ. The two internal clocks are 180° out of phase with one another [Redwine, 4:62-64; Fig. 3]. Thus, the memory device is able to out put serial data via output multiplexer 26 at twice the clock rate of the external clock Φ [Redwine, 7:17-26].

#14

Attention: Office of Petitions
Assistant Commissioner for Patents
Washington, D.C. 20231

FAX RECEIVED

JAN 3 0 2001

PETITIONS OFFICE

Sir:
      Transmitted herewith under 37 C.F.R. §1.53(d) is a Continued
Prosecution Application (CPA) for:

      Title: METHOD OF OPERATING A MEMORY DEVICE HAVING
             A VARIABLE DATA INPUT LENGTH

      Inventors: Michael Farmwald
                 Mark Horowitz

      Ser. No.:   09/492,982   Art Unit: 2818

      Filed: JANUARY 27, 2000   Examiner: T. NGUYEN

1.   **Petition under 37 C.F.R. §1.313(b)(5)**

      Submitted herewith is a petition pursuant to 37 CFR 1.313(b)(5) for
withdrawal from issue of the above identified application so that an
Information Disclosure Statement is considered in this Continued Prosecution
Application.

2.   **Correspondence Address:**

      Kindly address all communications to:

                                    Neil A. Steinberg, Esq.
                                    Rambus Inc.
                                    4440 El Camino Real
                                    Los Altos, California 94022

03/23/2001 VBROWN2 00000003 500998 09492982

                                    Telephone No. 650-947-5325
01 FC:103   108.00 CH   Facsimile No. 650-947-5001

Page 1

3. **FILING FEE**

Basic Fee . . . . $ 710.00

Additional Fees:

   Surcharge for more than 20 total claims (0) . . . . $ - 0 -

   Surcharge for more than 3 independent claims (0) . . . . . $ - 0 -

Total Filing Fee . . . . $ 710.00

5. **Manner of Payment:**

     [ ] A check payable to the Commissioner of Patents and Trademarks, in the amount of $ _____ is enclosed as payment of the Total Filing Fee.

     [XX] Please charge my Deposit Account No. 50-0998 in the amount of $ 710.00 to cover the above fees. A duplicate copy of this sheet is enclosed.

     [XX] The Commissioner is hereby authorized to charge any fees which may be required, or credit any overpayment to Deposit Account No. 50-0998. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

Date: January 29, 2001

Neil A. Steinberg
Reg. No. 34,735
650-947-5325

Page 2

#75

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
(Case No. P043D2C3C)

In the Application of:)
)
    FARMWALD et al.   )
)   Group
Serial No: 09/492,982   )   Art Unit: 2818
)
Filed: JANUARY 27, 2000   )   Before
)   Examiner: T. Nguyen
Title: METHOD OF OPERATING A MEMORY   )
         DEVICE HAVING A VARIABLE DATA   )
         INPUT LENGTH   )

Deputy Assistant Commissioner.
    for Patent Policy and Projects
Washington, DC 20231

Attention: Office of Petitions

FAX RECEIVED

JAN 3 0 2001

PETITIONS OFFICE

PETITION UNDER 37 C.F.R. §1.313(b)(5) FOR WITHDRAWAL FROM
ISSUE SO THAT INFORMATION CAN BE CONSIDERED IN A
CONTINUED PROSECUTION APPLICATION

Dear Sir:

    Applicants' hereby petition for withdrawal of the above-identified

application under 37 C.F.R. §1.313(b)(5) so that an Information

Disclosure Statement may be considered in a Continued Prosecution

Application (CPA). The above identified application has been allowed

and the issue fee has been paid. Recently, several documents have been

identified in a Notice of Opposition to European Patent 1 004 956,

which includes claims that are similar to claims in the parent patent.

(i.e., U.S. Patent 6,034,918) of the instant application.
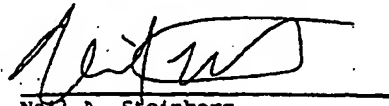
    Since the voluminous nature of Information Disclosure Statement

("IDS") and documents cited therein makes its submission by facsimile

impractical, a copy of the IDS is attached hereto and the ~~original~~ IDS

and documents cited therein are being filed by First Class Mail concurrently herewith.

Applicants hereby authorize charging deposit account no. 50-0998 the $130.00 petition fee under 37 C.F.R. §1.17(i). If there are any further charges associated with this submission; please charge deposit account no. 50-0998.

Respectfully submitted,

Date: January 29, 2001

Neil A. Steinberg
Reg. No. 34,735
650-947-5325

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
(Case No. P043D2C3C)

In the Application of:)
)
      FARMWALD et al.   )
) Group -
Serial No: 09/492,982   ) Art Unit:2818
)
Filed: JANUARY 27, 2000   ) Before
) Examiner: T. Nguyen
Title: METHOD OF OPERATING A MEMORY   )
         DEVICE HAVING A VARIABLE DATA)
         INPUT LENGTH   )

Box CPA

FACSIMILE COVER SHEET

DATE: January 30, 2001   FAX RECEIVED

TO: Office of Petitions   JAN 30 2001

FAX NUMBER: 703-308-6916   PETITIONS OFFICE

NO. OF PAGES: *10 attached*

MESSAGE
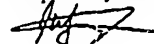
Attached is a petition under 37 CFR 1.313(b)(5), along with a 37 CFR 1.53(d) (CPA) application.

I hereby certify that the attached:

1. Transmittal-Request for a Continued Prosecution Application (CPA)
   (2 pages in duplicate)
2. Petition under 37 CFR 1.313 (b)(5) For Withdrawal From Issue So That Information
   Can Be Considered in an Information Disclosure Statement
   (2 pages in duplicate + 2 page attachment)

are being facsimile transmitted to the United States Patent and Trademark Office (Fax No.703-308-6916)
on January 30, 2001 in the above-referenced application.

                                    Respectfully submitted,

                                    Joe G. Moniz
                                    650-947-5336

UNITED STATES PATENT AND TRADEMARK OFFICE

Paper No. 16

NEIL A. STEINBERG, ESQ.
RAMBUS INC.
4440 EL CAMINO REAL
LOS ALTOS, CA 94022

COPY MAILED

MAR 0 2 2001

OFFICE OF PETITIONS
A/C P~~~ITS

In re Application of   :
Michael Farmwald et al   :
Application No. 09/492,982   :   ON PETITION
Filed: January 27, 2000   :
Attorney Docket No. P043D2C3C :

This is a decision on the petition under 37 CFR 1.313(b)(5),
filed January 30, 2001, which is being treated as a petition
under 37 CFR 1.313(c)(3) to withdraw the above-identified
application from issue after payment of the issue fee. See 1233
Official Gazette 54 (April 11, 2000).

The petition is **GRANTED**.

The above-identified application is hereby withdrawn from issue
in favor of a continued prosecution application (CPA) under 37
CFR 1.53(d).

*Petitioner is advised that the issue fee paid on December
12, 2000 in the parent application is not refundable nor can
it be applied towards any new Notice of Allowance which may
issue on the CPA filed January 30, 2001.*

Telephone inquiries should be directed to the undersigned at
(703) 305-8680.

The application is being forwarded to Technology Center AU 2818
for processing of the CPA.

Frances Hicks
Petitions Examiner
Office of Petitions
Office of the Deputy Commissioner
  for Patent Examination Policy

GP 2.818

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
(Case No. P043D2C3C)

In the Application of:

FARMWALD et al.

Serial No: 09/492,982

Filed: JANUARY 27, 2000

Title: METHOD OF OPERATING A MEMORY
DEVICE HAVING A VARIABLE DATA
INPUT LENGTH

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Group
Art Unit: 2816

Before
Examiner: T. Nguyen

RECEIVED MAR 13 2001 TECHNOLOGY CENTER 2800

Assistant Commissioner for Patents
Washington, DC 20231

INFORMATION DISCLOSURE STATEMENT

Dear Sir:

In compliance with the duty of disclosure set forth in 37 C.F.R. §1.56, submitted herewith is a modified Form PTO-1449, including a copy of all of the documents listed therein. An English translation has been obtained for one of the references and a copy of this translation is enclosed herewith.

Some of the references listed in the PTO-1449 have appeared in a communication from a foreign patent office in a related foreign application. A copy of that communication along with an English translation is also enclosed herewith.

It is respectfully requested that the Examiner make his consideration of the reference formally of record with the next Action. The Commissioner is hereby authorized to charge any fees which may be required in connection with this submission to Deposit Account No. 50-0998. A duplicate copy of this document is enclosed.

Date: _March 2_, 2001

Respectfully, submitted,

[signature]

Neil A. Steinberg
Reg. No. 34,735
650-947-5325

42

PTO-1449 (Modified)	ATTY. DOCKET NO. P043D2C3C	SERIAL NUMBER 09/492,982
U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	APPLICANT(S) FARMWALD ET AL.	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	FILING DATE JANUARY 27, 2000	GROUP ART UNIT 2818

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
~~—~~	~~5,034,964~~	~~Jul. 23, 1991~~	~~Khan et al.~~			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO
TN	SHO 58-192154	Nov. 9, 1983	Japan			NO
	SHO 63-34795	Feb. 15, 1988	Japan			NO
	SHO 61-107453	May 26, 1986	Japan			NO
	SHO 63-91766	April 22, 1988	Japan			YES
	SHO 62-16289	Jan. 24, 1987	Japan			NO
TNT	SHO 61-160556	Oct. 4, 1986	Japan			NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER TAN T. NGUYEN	DATE CONSIDERED 05/17/01

EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant.

Ms. Michiko Sites
RAMBUS INC.
4440 El Camino Real
Los Altos, CA 94022

RECEIVED
MAR 13 2001
TECHNOLOGY CENTER 2800

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
(Atty. Docket No. P043D2C3C)

APPLICANT: FARMWALD ET AL.   FILED: JANUARY 27, 2000

SERIAL NO.: 09/492,982

TITLE: METHOD OF OPERATING A MEMORY DEVICE HAVING A
          VARIABLE DATA INPUT LENGTH

RECEIPT OF THE FOLLOWING PAPERS IS ACKNOWLEDGED

1. Information Disclosure Statement (1 page + 1 copy thereof + PTO-1449
   (1 page)) + REFERENCES

DATE: MARCH 5, 2001   ATTY: NAS

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
(Case No. P043D2C3C)

In the Application of:)
)
FARMWALD et al.)
) Group
Serial No: 09/492,982) Art Unit: 2818
)
Filed: JANUARY 27, 2000) Before
) Examiner: T. Nguyen
Title: METHOD OF OPERATING A MEMORY)
DEVICE HAVING A VARIABLE DATA)
INPUT LENGTH)

Assistant Commissioner for Patents
Washington, DC 20231

INFORMATION DISCLOSURE STATEMENT

Dear Sir:

In compliance with the duty of disclosure set forth in 37 C.F.R. §1.56, submitted herewith is a modified Form PTO-1449, including a copy of all of the documents listed therein.

The documents listed in the PTO-1449 have been recently identified in a pending U.S. District Court For Eastern District of Virginia case, namely in Rambus Inc. v. Infineon Technologies A.G., et al., as prior art against the inventions claimed in U.S. Patent 6,034,918, the parent of the instant application. An explicit reference to these documents is made on pages 18-21 in the DEFENDANT INFINEON TECHNOLOGIES AG'S FIRST SUPPLEMENTAL RESPONSES TO PLAINTIFF'S INTERROGATORIES NOS. 3, 5 and 6 (hereinafter the "SUPPLEMENTAL RESPONSE"). A copy of the SUPPLEMENTAL RESPONSE is included herewith.

It is respectfully requested that the Examiner make his consideration of these references formally of record with the next Action. The Commissioner is hereby authorized to charge any fees which may be required in connection with this submission to Deposit Account No. 50-0998. A duplicate copy of this document is enclosed.

Respectfully submitted,

Date: Feb. 8, 2001

Neil A. Steinberg
Reg. No. 34,735
650-947-5325

PTO-1449 (Modified)	ATTY. DOCKET NO. P043D2C3C	SERIAL NUMBER 09/492,982
U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	APPLICANT(S) FARMWALD ET AL.	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	FILING DATE JANUARY 27, 2000	GROUP ART UNIT 2818

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
TNI	4,482,999	11/13/84	Janson et al.	37°	л52	
	4,835,674	05/30/89	Collins et al.	7°9	214	
	5,193,193	03/09/93	Iyer	710	117	
	5,179,667	01/12/93	Iyer	711	167	
	4,926,385	05/15/90	Fujishima et al.	365	230.03	
	4,566,099	01/21/86	Magerl	370	509	
	4,803,621	02/07/89	Kelly	711	5	
	4,589,108	05/13/86	Billy	37°	503	
	4,870,622	09/26/89	Aria et al.	365	230.02	
	5,134,699	07/28/92	Aria et al.	7°	35	
	4,878,166	10/31/89	Johnson et al.	710	127	
	4,849,965	07/18/89	Chomel et al.	370	л36	
TNI	4,851,990	07/25/89	Johnson et al.	710	129	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER TAN . NGUYEN	DATE CONSIDERED 05/17/01

EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant.

PTO-1449 (Modified)	ATTY. DOCKET NO. P043D2C3C	SERIAL NUMBER 09/492,982
U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	APPLICANT(S) FARMWALD ET AL.	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	FILING DATE JANUARY 27, 2000	GROUP ART UNIT 2818

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
7N T	4,048,673	09/13/77	Hendrie et al.	710	129	
	4,748,617	05/31/88	Drewlo	359	121	
	4,435,762	03/06/84	Milligan et al.	710	6	
	4,839,801	06/13/89	Nicely et al.	710	35	
	4,949,301	08/14/90	Joshi et al.	711	100	
	4,047,246	09/06/77	Kerilenevich et al.	710	61	
	5,029,124	07/02/91	Leahy et al.	710	105	
TN T	4,625,307	11/25/86	Tulpule et al.	370	402	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER Tan T. Nguyen	DATE CONSIDERED 05/17/01

EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant.

IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF VIRGINIA
(Richmond Division)

RAMBUS INC. Plaintiff, v. INFINEON TECHNOLOGIES AG, et al., Defendants.	Civil Action No. 3:00CV524

DEFENDANT INFINEON TECHNOLOGIES AG 'S
FIRST SUPPLEMENTAL RESPONSES TO PLAINTIFF'S
INTERROGATORIES NOS. 3, 5 and 6

Pursuant to Federal Rule of Civil Procedure 33, Plaintiff Infineon Technologies AG

("Infineon") hereby makes the following supplemental responses to Plaintiff Rambus, Inc.'s

("Rambus"") Interrogatories Nos. 3, 5 and 6. Each response herein is made subject to and without

waiver of Infineon's previously-stated General and Specific Objections. Pursuant to Federal Rule of

Civil Procedure 26(e), Infineon reserves the right to supplement its responses or document

production if it learns of additional responsive information.

SUPPLEMENTAL RESPONSES

INTERROGATORY NO. 3:

Identify each and every customer of Infineon that has purchased or is purchasing Infineon SDRAMs, DDR SDRAMs, or SGRAMs, or any modules that contain any such devices, within the United States or for inclusion in products sold or offered for sale in the United States, identifying the devices, modules or chip sets purchased and the date of purchase.

SUPPLEMENTAL RESPONSE TO INTERROGATORY NO. 3:

To the extent any consumers are identified in response to Interrogatory No. 3, Infineon responds pursuant to Fed. R. Civ. P. 33(d) that the answer to this interrogatory may be derived or ascertained from the business records of Infineon that have been produced in this action. Such documents include I 023284 - I 023309, I 089866 - I 08911 and I 141447 - I 141514.

INTERROGATORY NO. 5:

For each and every Infineon product or device accused of infringement in this action, identify on a claim chart (on a product-by-product basis) each limitation of each claim of the patents-in-suit that Infineon contends is not met by each such product or device, the basis for Infineon's contention that the limitation is not met literally or under the doctrine of equivalents, and all portions of the patents-in-suit and related prosecution file and/or prior art references that Infineon asserts support its contention.

SUPPLEMENTAL RESPONSE TO INTERROGATORY NO. 5:

Noninfringement of patent claims depends, in part, on the interpretation of claim language in the asserted claims. Claim construction is a question of law for the Court. In this case, the Court has not yet construed any claims of the patents-in-suit. Accordingly, Infineon reserves its rights to supplement or amend its responses to this interrogatory once the Court rules on the interpretation of the claim language in the asserted claims of the patents-in-suit. In addition, Rambus bears the burden of proof for infringement, but has not identified with specificity which of the accused products infringe each asserted claim. Accordingly, pursuant to Infineon's interpretation and

-2-

understanding of the asserted claims and Rambus' generic infringement contentions, the products accused by Rambus do not infringe for at least the following reasons:

A.   U.S. Patent No. 5,953,263

In response to Infineon's Interrogatory No. 1, Rambus accused Infineon's SDRAMs, DDR SDRAMs and SGRAMs of literally infringing claims 1-5, 14-19, 21, 23-25, 27-28 and 30-33 of the '263 patent. Rambus does not, however, identify any specific circuitry or methods of operating a semiconductor memory device that allegedly infringe particular asserted claims. Infineon's investigation to date reveals that none of the accused products infringe the asserted claims of the '263 patent for one or more of the following reasons: 1) the accused products do not respond to read requests; 2) the accused products do not contain a programmable register to store a value that is representative of a delay time after which the memory device responds to a read request; 3) the accused products do not contain a programmable register to store a value that is representative of a number of clock cycles of an external clock to transpire before data is output onto an external bus in response to a read request; 4) the accused products do not include output drivers to output data onto an external bus after a number of clock cycles of an external clock transpire; 5) the accused products do not output data onto an external bus synchronously with respect to an external clock; 6) the accused products do not contain a programmable register to store a value representative of a number of clock cycles of a clock to transpire before data is output onto a bus in response to a read request; 7) the accused products do not include output drivers to output data onto a bus after a number of clock cycles of a clock transpire; 8) the accused products do not output data onto a bus synchronously with respect to a clock; 9) the accused products do not perform methods that include the steps of receiving and storing a time delay value in a programmable register that is representative of a number of clock cycles of an external clock to transpire before data is output onto an external

-3-

bus in response to a read request or a transaction request; and 10) the accused products do not

perform methods that include the step of selecting one of a plurality of time delays after which the

memory device provides data in response to a read request. In addition, the accused Infineon

products practice the prior art. Thus, to the extent that Rambus attempts to expand the asserted

claims to cover the accused Infineon products, those claims are invalid over the prior art.

B.   U.S. Patent No. 5,954,804

In response to Infineon's Interrogatory No. 1, Rambus accused Infineon's SDRAMs,

DDR SDRAMs and SGRAMs of infringing claim 26 of the '804 patent. Rambus does not, however,

identify any specific circuitry that allegedly infringes that particular claim. Infineon's investigation to

date reveals that none of the accused products infringe the asserted claim of the '804 patent for one

or more of the following reasons: 1) the accused products do not output data on an external bus

synchronously with respect to first and second external clock signals; 2) the accused products do not

respond to read requests, and do not contain an internal register to store a value which is

representative of a number of clock cycles to transpire before responding to a read request; 3) the

accused products do not contain delay locked loop circuitry to generate an internal clock signal using

first and second external clock signals; 4) the accused products do not have interface circuitry,

coupled to an external bus to receive a read request; and 5) the accused products do not output data

on the external bus in response to an internal clock signal synchronously with respect to first and

second external clock signals and in accordance with a value stored in a first internal register that is

representative of a number of clock cycles to transpire before the device responds to a read request.

In addition, the accused Infineon products practice the prior art. Thus, to the extent that Rambus

attempts to expand the asserted claim to cover the accused Infineon products, that claim is invalid

over the prior art.

-4-

C.   U.S. Patent No. 6,032,214

In response to Infineon's Interrogatory No. 1, Rambus accused Infineon's SDRAMs,
DDR SDRAMs and SGRAMs of infringing claims 1, 2, 4, 6, 9-11, 14-16, 18, 19, 21, 24-26 and 29
of the '214 patent.   Rambus does not, however, identify any specific circuitry or methods of
operating a synchronous memory device that allegedly infringe particular claims.   Infineon's
investigation to date reveals that none of the accused products infringe the asserted claims of the '214
patent for one or more of the following reasons: 1) the accused Infineon products do not provide first
block size information to a memory device in the form of a binary code or otherwise; 2) the accused
Infineon products do not issue first or second read requests to a memory device; 3) the accused
Infineon products do not have first and second external clock signals; 4) the accused devices do not
output data on an external bus synchronously with respect to first and second external clock signals;
5) the accused products do not respond to read requests; 6) the accused products do not store a code
in an access-time register that is representative of a number of clock cycles; and 7) and the accused
Infineon products are not automatically precharged after executing a read request. In addition, the
accused Infineon products practice the prior art. Thus, to the extent that Rambus attempts to expand
the asserted claims to cover the accused Infineon products, those claims are invalid over the prior art.

D.   U.S. Patent No. 6,034,918

In response to Infineon's Interrogatory No. 1, Rambus accused Infineon's SDRAMs,
DDR SDRAMs and SGRAMs of infringing claims 1, 2, 6, 8-9, 13, 15-20, 24, 25, 29-31, 33 and 34
of the '918 patent. Rambus does not, however, identify any specific circuitry or methods of operating
and/or controlling a synchronous memory device that allegedly infringe particular asserted claims.
Infineon's investigation to date reveals that none of the accused products infringe the asserted claims
of the '918 patent for one or more of the following reasons: 1) the accused products do not provide

-5-

first or second block size information to a memory device, wherein the block size information defines an amount of data; 2) the accused products do not issue first or second read requests to a memory device; 3) the accused products do not issue first or second write requests to a memory device; 4) the accused products do not output data corresponding to first or second block size information onto the bus synchronously with respect to an external clock signal; 5) the accused products do not provide or store a code which is representative of a delay time to transpire before data is output onto the bus after receipt of a read request; 6) the accused products do not receive first block size information from a bus controller, wherein the first block size information defines a first amount of data to be output by the memory device onto a bus in response to a read request; 7) the accused products do not output a first amount of data corresponding to first block size information, in response to a first read request, onto a bus synchronously with respect to an external clock signal; 8) the accused products do not output a first amount of data corresponding to first block size information in response to a second read request onto a bus synchronously with respect to an external clock signal; 9) the accused products do not input a first amount of data corresponding to first block size information in response to a first write request from a bus synchronously with respect to an external clock signal; 10) the accused products do not store a value in a time delay register, the value being representative of a number of external clock cycles to transpire; 11) the accused products do not receive block size information from a bus controller wherein the block size information defines a first amount of data to be output by the memory device onto the bus in response to a read request; 12) the accused products do not output a first amount of data corresponding to block size information in response to a first read request; 13) the accused products do not output data synchronously with respect to an external clock signal during a plurality of clock cycles of an external clock signal in accordance with a value stored in a time delay register; and 14) the accused Infineon

-6-

products do not use a DLL to generate an internal clock signal. In addition, the accused Infineon products practice the prior art. Thus, to the extent that Rambus attempts to expand the asserted claims to cover the accused Infineon products, those claims are invalid over the prior art.

INTERROGATORY NO. 6:

      If Infineon contends that any or all of the claims of the patents-in-suit are invalid or unenforceable, state the basis for such contention by identifying each such patent and claim, each fact underlying such contention, including the identification of any alleged prior act, the individuals who have knowledge of the facts underlying such contention, and all documents related to such contention.

SUPPLEMENTAL RESPONSE TO INTERROGATORY NO. 6:

      Based on its investigation to date, each of the asserted claims of the patents-in-suit are invalid and/or unenforceable for one or more of the following reasons:

      The patents-in-suit are unenforceable due to patent misuse and estoppel due to Rambus' misconduct at JEDEC because throughout its tenure as a JEDEC member, under the policies and rules of JEDEC, Rambus was obligated to disclose any patents or patent applications that might be involved in the work of any of the committee meetings that its representatives attended. As of 1992, Rambus believed that its pending patent applications covered the SDRAM technology being discussed for standardization by JEDEC Committee 42.3. Further, pursuant to its patent strategy, at various times during its tenure as a member of JEDEC, Rambus filed continuation patent applications for the express purpose of filing claims to track the SDRAM technology being discussed at the JEDEC meetings its representatives attended. Rambus attended no less than 15 JEDEC committee 42.3 meetings during which SDRAM standardization was discussed, but never disclosed to the JEDEC members that it had pending patent applications that it believed covered the work being discussed by the committee nor did it disclose that it intended

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and did file claims to cover the work of the committee. Instead, the only disclosures of intellectual property rights by Rambus were patents that did not relate to the work being done by the committee. In reliance of Rambus' silence with regard to patents and patent applications that might relate to the SDRAM standardization work, JEDEC and its members, including Infineon, unknowingly adopted SDRAM standards that Rambus now claims are covered by its patents. Further Infineon has made substantial investments in developing, manufacturing and selling SDRAM and DDR SDRAM products that are compatible with the JEDEC standards, believing these standards to be open standards. The details of the factual basis for Infineon's affirmative defense that the patents-in-suit are unenforceable due to equitable estoppel and patent misuse are set forth in paragraphs 74-194 of Infineon's Answer and Counterclaims to Rambus' First Amended Complaint, which are incorporated by reference in their entirety in this response. Moreover, Rambus' delay in filing the patent applications that contain the asserted claims until after it terminated its membership in JEDEC constitutes laches.

A.   U.S. Patent No. 5,953,263

The '263 patent is also unenforceable due to inequitable conduct during prosecution of the patent application that matured into the '263 patent and due to inequitable conduct during the prosecution of Application Serial No. 07/510,898 ("the '898 application") and subsequent patent applications related to the '263 patent, including patent applications through which the '263 patent claims priority to the '898 application, for failure to cite, *inter alia*, the following references to the PTO:

1.   U.S. Patent No. 5,140,688; and

2.   Documents published during the development of specifications for the Scalable Coherent Interface Project, IEEE P1596 (collectively "SCI publications"), including:

a.   David B. Gustavson et al.," The Scalable Coherent Interface Project
      (Superbus)", draft of August 22, 1988;

b.   David B. Gustavson, "Scalable Coherent Interface", November 1988, (paper
      to appear at COMPCON Spring 1989);

c.   David V. James, "Scalable I/O Architecture for Buses", November 1988,
      (paper to appear at COMPCON Spring 1989);

d.   David V. James, "P1596: SCI, A Scalable Coherent Interface", November
      1988, (transparencies);

e.   Knut Alnes, "SCI: A Proposal For SCI Operation", November 1988;

f.   Knut Alnes, "SCI: A Proposal For SCI Operation", January 1989;

g.   Bjørn O. Bakka et al., "SCI: Logical Level Proposals", January 1989;

h.   Ernst H. Kristiansen et al., "Scalable Coherent Interface", February 1989,
      (paper to appear in Eurobus Conference Proceedings, Munich, May 1989);

i.   Morten Schanke, "Proposal For Clock Distribution in SCI", May 1989; and

j.   Ernst H. Kristiansen et al., "Scalable Coherent Interface", Eurobus, London,
      September 1989.

      Claims 1, 18, 24-25 and 27 are invalid under 35 U.S.C. § 102 and/or § 103, in view
of the following references, either alone or in combination with either one or more of the following

listed references and/or the general knowledge of one of skill in the art:

1.   U.S. Patent No. 3,950,735;

2.   Japanese Patent Application 54-160587;

3.   U.S. Patent No. 4,445,204;

4.   Japanese Patent Application 55-89232;

5.   Japanese Patent Application 58-186919;

6.   U.S. Patent No. 4,858,113;

7.   U.S. Patent No. 4,953,128;

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8.   U.S. Patent No. 5,140,688;

9.   Japanese Patent Application 62-51509;

10.   Japanese Patent Application 62-71428;

11.   Japanese Patent Application 62-185253;

12.   ICs For Entertainment Electronics – Picture-in-Picture System, as described in data sheets of SDA 9087 and SDA 9088 published by Siemens; and

13.   Giga Bit Logic 12G014 data sheet "256x4 Bit Registered, Self-Timed Static RAM, 2.5 ns Cycle Time," 1989 GaAs IC Data Book & Designer's Guide.

Claims 2-3, 14-15 and 30-31 are invalid under 35 U.S.C. § 102 and/or § 103, in view of the following references, either alone or in combination with either one or more of the following listed references and/or the general knowledge of one of skill in the art:

1.   U.S. Patent No. 3,950,735;

2.   Japanese Patent Application 54-160587;

3.   U.S. Patent No. 4,445,204;

4.   Japanese Patent Application 55-89232;

5.   Japanese Patent Application 58-186919;

6.   U.S. Patent No. 4,858,113;

7.   U.S. Patent No. 4,953,128;

8.   U.S. Patent No. 5,140,688;

9.   Japanese Patent Application 62-71428;

10.   Japanese Patent Application 62-185253;

11.   ICs For Entertainment Electronics – Picture-in-Picture System, as described in data sheets of SDA 9087 and SDA 9088 published by Siemens; and

12.   Giga Bit Logic 12G014 data sheet "256x4 Bit Registered, Self-Timed Static RAM, 2.5 ns Cycle Time," 1989 GaAs IC Data Book & Designer's Guide.

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Claims 4 and 23 are invalid under 35 U.S. C. § 102 and/or § 103, in view of the

following references, either alone or in combination with either one or more of the following listed

references and/or the general knowledge of one of skill in the art:

1.   Japanese Patent Application 54-160587;

2.   U.S. Patent No. 4,445,204;

3.   Japanese Patent Application 55-89232;

4.   Japanese Patent Application 58-186919;

5.   U.S. Patent No. 4,858,113;

6.   U.S. Patent No. 4,953,128;

7.   U.S. Patent No. 5,140,688;

8.   Japanese Patent Application 62-51509;

9.   Japanese Patent Application 62-71428;

10.   Japanese Patent Application 62-185253; and

11.   ICs For Entertainment Electronics – Picture-in-Picture System, as described in data
      sheets of SDA 9087 and SDA 9088 published by Siemens.

Claims 5, 19, 21 and 28 are invalid under 35 U.S. C. § 102 and/or § 103, in view of

the following references, either alone or in combination with either one or more of the following listed

references and/or the general knowledge of one of skill in the art:

1.   Japanese Patent Application 54-160587;

2.   Japanese Patent Application 55-89232;

3.   Japanese Patent Application 58-186919;

4.   U.S. Patent No. 4,858,113;

5.   U.S. Patent No. 4,953,128;

6.   U.S. Patent No. 5,140,688;

-11-

7.   Japanese Patent Application 62-51509;

8.   Japanese Patent Application 62-71428; and

9.   ICs For Entertainment Electronics – Picture-in-Picture System, as described in data sheets of SDA 9087 and SDA 9088 published by Siemens.

Claims 16 and 32 are invalid under 35 U.S.C. § 102 and/or § 103, in view of the following references, either alone or in combination with either one or more of the following listed references and/or the general knowledge of one of skill in the art:

1.   Japanese Patent Application 54-160587;

2.   U.S. Patent No. 4,445,204;

3.   Japanese Patent Application 55-89232;

4.   Japanese Patent Application 58-186919;

5.   U.S. Patent No. 4,858,113;

6.   U.S. Patent No. 4,953,128;

7.   U.S. Patent No. 5,140,688;

8.   Japanese Patent Application 62-71428;

9.   Japanese Patent Application 62-185253; and

10.   ICs For Entertainment Electronics – Picture-in-Picture System, as described in data sheets of SDA 9087 and SDA 9088 published by Siemens.

Claims 17 and 33 are invalid under 35 U.S.C. § 102 and/or § 103, in view of the following references, either alone or in combination with either one or more of the following listed references and/or the general knowledge of one of skill in the art:

1.   Japanese Patent Application 54-160587;

2.   Japanese Patent Application 55-89232;

3.   Japanese Patent Application 58-186919;

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4.   U.S. Patent No. 4,858,113;

5.   U.S. Patent No. 4,953,128;

6.   U.S. Patent No. 5,140,688;

7.   Japanese Patent Application 62-71428; and

8.   ICs For Entertainment Electronics – Picture-in-Picture System, as described in data sheets of SDA 9087 and SDA 9088 published by Siemens.

The asserted claims of the '263 patent are also invalid under 35 U.S.C. § 112 for omitting elements that one of ordinary skill in the art would understand as being essential to the alleged invention as originally disclosed, and for lack of enablement and/or support in the specification to the extent that those claims are broadly interpreted to cover Infineon's accused products, including expansive interpretations of terms and/or phrases such as: "read request," "transaction request," "to output data on the bus, in response to the read request, synchronously with respect to an external clock," "the value is representative of a number of clock cycles of the external clock," "a programmable register to store a value which is representative of a number of clock cycles of an external clock," "wherein the output drivers output data on the bus after the number of clock cycles of the external clock transpire," "wherein the value is representative of a fraction or a whole number of clock cycles of the external clock" and "receiving a time delay value, wherein the delay value is representative of a number of clock cycles of an external clock."

B.   U.S. Patent No. 5,954,804

The '804 patent is also unenforceable due to inequitable conduct during prosecution of the patent application that matured into the '804 patent and due to inequitable conduct during the prosecution of Application Serial No. 07/510,898 ("the '898 application") and subsequent patent applications related to the '804 patent, including patent applications through which the '804 patent

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claims priority to the '898 application, for failure to cite, *inter alia*, the following references to the

PTO:

1.   U.S. Patent No. 4,998,262; and

2.   Documents published during the development of specifications for the Scalable
Coherent Interface Project, IEEE P1596, including the publications listed in Section
A as 2(a)-(j).

Claim 26 of the '804 patent is invalid under 35 U.S.C. § 102 and/or § 103, in view of

the above references and the references listed below, either alone or in combination with each other

and/or the general knowledge of one of skill in the art:

1.   U.S. Patent No. 3,950,735;

2.   Japanese Patent Application 54-160587;

3.   U.S. Patent No. 4,445,204;

4.   Japanese Patent Application 55-89232;

5.   Japanese Patent Application 58-186919;

6.   U.S. Patent No. 4,858,113;

7.   U.S. Patent No. 4,953,128;

8.   U.S. Patent No. 5,140,688;

9.   Japanese Patent Application 62-51509;

10.   Japanese Patent Application 62-71428;

11.   Japanese Patent Application 62-185253;

12.   ICs For Entertainment Electronics – Picture-in-Picture System, as described in data
sheets of SDA 9087 and SDA 9088 published by Siemens;

13.   Giga Bit Logic 12G014 data sheet "256x4 Bit Registered, Self-Timed Static RAM,
2.5 ns Cycle Time," 1989 GaAs IC Data Book & Designer's Guide.

14.   U.S. Patent No. 4,338,569; and

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15.   U.S. Patent No. 5,361,277.

Claim 26 of the '804 patent is also invalid under 35 U.S.C. § 112 for lack of

enablement and/or support in the specification to the extent that those claims are broadly interpreted

to cover Infineon's accused products, including expansive interpretations of terms and/or phrases such

as: "read request," "first and second external clock signals," "interface circuitry, coupled to the

external bus to receive a read request" and "outputs data on an external bus synchronously with

respect to first and second external clock signals."

C.   U.S. Patent No. 6,032,214

The '214 patent is also unenforceable due to inequitable conduct during prosecution

of the patent application that matured into the '214 patent and due to inequitable conduct during the

prosecution of Application Serial No. 07/510,898 ("the '898 application") and subsequent patent

applications related to the '214 patent, including patent applications through which the '214 patent

claims priority to the '898 application, for failure to cite, *inter alia*, the following references to the

PTO:

1.   U.S. Patent No. 3,771,145; and

2.   Documents published during the development of specifications for the Scalable
      Coherent Interface Project, IEEE P1596, including the publications listed in Section
      A as 2(a)-(j).

The asserted claims of the '214 patent are invalid under 35 U.S.C. § 102 and/or § 103,

in view of the above references and the references listed below, either alone or in combination with

each other and/or the general knowledge of one of skill in the art:

1.   Japanese Patent Application 63-239676;

2.   U.S. Patent No. 4,763,249;

3.   Unisys JEDEC Presentation - December 6, 1988;

-15-

4.   Kalter et. al., *A 50ns 16 Mb DRAM with a 10ns Data Rate*, 1990 IEEE International
       Solid-State Circuits Conference, pp. 232-33, 303, February 16, 1990;

5.   Kalter et. al., *A 50ns 16 Mb DRAM with a 10ns Data Rate and On-Chip ECC*, 1990
       IEEE Journal of Solid-State Circuits, vol. 25, no. 5, pp. 1118-28, October 1990;

6.   Japanese Patent Application 63-142445;

7.   *Fast Packet Bus for Microprocessor Systems with Caches*, IBM Technical Disclosure
       Bulletin, vol. 31, no. 8, pp. 279-82, January 1989;

8.   Watanabe, *High-Density SRAMs*, 1987 IEEE International Solid-State Circuits
       Conference, pp. 266-67; February 27, 1987;

9.   Japanese Patent Application 61-72350;

10.   U.S. Patent No. 5,134,699;

11.   U.S. Patent No. 4,315,308

12.   ICs For Entertainment Electronics – Picture-in-Picture System, as described in data
       sheets of SDA 9087 and SDA 9088 published by Siemens;

13.   Anceau, *A Synchronous Approach for Clocking VLSI Systems*, IEEE Journal of
       Solid-State Circuits, Vol. SC-17, No. 1, February 1982;

14.   German Laid-Open Patent Application DE 3733554 A1, published April 21, 1988;

15.   Motorola's MC88200 chip;

16.   Ogiue et al., *13-ns, 500-mW, 64-kbit ECL RAM Using HI-BICMOS Technology*,
       IEEE Journal of Solid-State Circuits, Vol. SC-21, No. 5, October 1986;

17.   U.S. Patent No. 4,205,500;

18.   U.S. Patent No. 4,803,621;

19.   U.S. Patent No. 4,870,622;

20.   U.S. Patent No. 4,926,385;

21.   U.S. Patent No. 4,927,791;

22.   U.S. Patent No. 4,480,307;

23.   U.S Patent No. 5,179,667;

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24.   U.S. Patent No. 4,773,066;

25.   U.S. Patent No. 4,851,990;

26.   U.S. Patent No. 4,878,166

27.   U.S. Patent No. 4,528,661;

28.   U.S. Patent No. 4,849,965;

29.   U.S. Patent No. 4,435,762;

30.   U.S. Patent No. 4,949,301;

31.   U.S. Patent No. 4,835,674;

32.   U.S. Patent No. 4,839,801;

33.   U.S. Patent No. 4,589,108;

34.   U.S. Patent No. 5,029,124;

35.   U.S. Patent No. 4,625,307;

36.   U.S. Patent No. 4,748,617;

37.   U.S. Patent No. 5,193,193;

38.   U.S. Patent No. 4,482,999;

39.   U.S. Patent No. 4,566,099;

40.   U.S. Patent No. 4,047,246;

41.   U.S. Patent No. 4,048,673;

42.   U.S. Patent No. 4,519,034;

43.   Voelker, IEEE Spectrum, Feb. 1987;

44.   Dix et al, IBM Journal of Research and Development Vol 26, #4 July 1982;

45.   Grossman, IBM Systems Journal, Vol. 24, No. S3/4 1985; and

46.   U.S. Patent No. 3,950,735.

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The asserted claims of the '214 patent are also invalid under 35 U.S.C. § 112 for lack of enablement and/or support in the specification to the extent that those claims are broadly interpreted to cover Infineon's accused products, including expansive interpretations of terms and/or phrases such as: "read request," "write request," outputting data "synchronously with respect to a first and second external clock signal wherein a first portion of the first amount of data is output synchronously with respect to the first external clock signal and a second portion of the first amount of data is output synchronously with respect to the second external clock signal," and "storing a code in an access-time register, the code being representative of a number of clock cycles of the first and second external clock signals to transpire before data is output."

D.   U.S. Patent No. 6,034,918

The '918 patent is also unenforceable due to inequitable conduct during prosecution of the patent application that matured into the '918 patent and due to inequitable conduct during the prosecution of Application Serial No. 07/510,898 ("the '898 application") and subsequent patent applications related to the '918 patent, including patent applications through which the '918 patent claims priority to the '898 application, for failure to cite, *inter alia*, the following references to the PTO:

1.   U.S. Patent No. 3,771,145; and

2.   Documents published during the development of specifications for the Scalable Coherent Interface Project, IEEE P1596, including the publications listed in Section A as 2(a)-(j).

The asserted claims of the '918 patent are invalid under 35 U.S.C. § 102 and/or § 103, in view of the above references and the references listed below, either alone or in combination with each other and/or the general knowledge of one of skill in the art:

1.   Japanese Patent Application 63-239676;

-18-

2.   U.S. Patent No. 4,763,249;

3.   Unisys JEDEC Presentation - December 6, 1988;

4. _   Kalter et. al., *A 50ns 16Mb DRAM with a 10ns Data Rate*, 1990 IEEE International
        Solid-State Circuits Conference, pp. 232-33, 303, February 16, 1990;

5.   Kalter et. al., *A 50ns 16Mb DRAM with a 10ns Data Rate and On-Chip ECC*, 1990
        IEEE Journal of Solid-State Circuits, vol. 25, no. 5, pp. 1118-28, October 1990;

6.   Japanese Patent Application 63-142445;

7.   *Fast Packet Bus for Microprocessor Systems with Caches*, IBM Technical Disclosure
        Bulletin, vol. 31, no. 8, pp. 279-82, January 1989;

8.   Watanabe, *High-Density SRAMs*, 1987 IEEE International Solid-State Circuits
        Conference, pp. 266-67; February 27, 1987;

9.   Japanese Patent Application 61-72350;

10.   U.S. Patent No. 5,134,699;

11.   U.S. Patent No. 4,315,308

12.   ICs For Entertainment Electronics – Picture-in-Picture System, as described in data
        sheets of SDA 9087 and SDA 9088 published by Siemens;

13.   Anceau, *A Synchronous Approach for Clocking VLSI Systems*, IEEE Journal of
        Solid-State Circuits, Vol. SC-17, No. 1, February 1982;

14.   German Laid-Open Patent Application DE 3733554 A1, published April 21, 1988;

15.   Motorola's MC88200 chip;

16.   Ogiue et al., *13-ns, 500-mW, 64-kbit ECL RAM Using HI-BICMOS Technology*,
        IEEE Journal of Solid-State Circuits, Vol. SC-21, No. 5, October 1986;

17.   U.S. Patent No. 4,205,500;

18.   U.S. Patent No. 4,803,621;

19.   U.S. Patent No. 4,870,622;

20.   U.S. Patent No. 4,926,385;

21.   U.S. Patent No. 4,927,791;

-19-

22.   U.S. Patent No. 4,480,307;

23.   U.S. Patent No. 5,179,667;

24.   U.S. Patent No. 4,773,066;

25.   U.S. Patent No. 4,851,990;

26.   U.S. Patent No. 4,878,166

27.   U.S. Patent No. 4,528,661;

28.   U.S. Patent No. 4,849,965;

29.   U.S. Patent No. 4,435,762;

30.   U.S. Patent No. 4,949,301;

31.   U.S. Patent No. 4,835,674;

32.   U.S. Patent No. 4,839,801;

33.   U.S. Patent No. 4,589,108;

34.   U.S. Patent No. 5,029,124;

35.   U.S. Patent No. 4,625,307;

36.   U.S. Patent No. 4,748,617;

37.   U.S. Patent No. 5,193,193;

38.   U.S. Patent No. 4,482,999;

39.   U.S. Patent No. 4,566,099;

40.   U.S. Patent No. 4,047,246;

41.   U.S. Patent No. 4,048,673;

42.   U.S. Patent No. 4,519,034;

43.   Voelker, IEEE Spectrum, Feb. 1987;

44.   Dix et al, IBM Journal of Research and Development Vol 26, #4 July 1982;

-20-

45.   Grossman, IBM Systems Journal, Vol. 24, No. S3/4 1985; and .

46.   U.S. Patent No. 3,950,735.

The asserted claims of the '918 patent are also invalid under 35 U.S.C. § 112 for lack of enablement and/or support in the specification to the extent that those claims are broadly interpreted to cover Infineon's accused products, including expansive interpretations of terms and/or phrases such as: "read request," "write request," "providing first block size information to the memory device, wherein the first block size information defines a first amount of data," "issuing a first read request," "outputs the first amount of data corresponding the first block size information synchronously with respect to an external clock signal," "issuing a second read request," "providing a code which is representative of a delay time to transpire before data is output onto the bus after receipt of a read request," "receiving the external clock signal wherein the first amount of data corresponding to the first block size information is output in accordance with the delay time," "wherein the first amount of data corresponding to the first block size information is output synchronously during a plurality of clock cycles," "receiving first block size information from a bus controller, wherein the first block size information defines a first amount of data to be output," "in response to a read request," "outputting the first amount of data corresponding to the first block size information, in response to the first read request, onto the bus synchronously with respect to the external clock signal," "receiving a second read request," "outputting the first amount of data corresponding to the first block size information, in response to the second read request, onto the bus synchronously with respect to the external clock signal," "receiving a first write request," and "inputting the amount of data corresponding to the second block size information, in response to the second write request, from the bus synchronously with respect to the external clock signal."

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Dated: December 4, 2000

_____

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INFINEON TECHNOLOGIES HOLDING NORTH AMERICA INC.

-22-

CERTIFICATE OF SERVICE
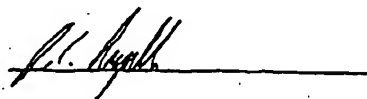
I certify that on this 4th day of December, 2000, a copy of the foregoing
DEFENDANT INFINEON TECHNOLOGIES AG'S FIRST SUPPLEMENTAL RESPONSES
TO PLAINTIFF'S INTERROGATORIES NOS. 3, 5 and 6 was sent to Counsel for Rambus Inc.
as listed below:

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-23-

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
(Case No. P043D2C3C)

In the Application of:)
)
    FARMWALD, ET AL.)
)
Serial No.: 09/492,982)
)
Filed: JANUARY 27, 2000)
)
Title: METHOD OF OPERATING A MEMORY)
    DEVICE HAVING A VARIABLE DATA)
    INPUT LENGTH)
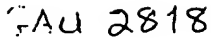
Assistant Commissioner for Patents
Washington, DC 20231

Certificate of Mailing Under 37 CFR 1.8

I hereby certify that the attached 1) Information Disclosure Statement (1 page

and 1 copy thereof + 2 page PTO-1449 attached + references cited therein) is/are

being deposited with the United States Postal Service with sufficient postage as first

class U.S. mail in an envelope addressed to:

        Assistant Commissioner for Patents
        Washington, D.C. 20231

On February 8, 2001.

(Signature)

Michiko Sites

(Print Name of Person Signing Certificate)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
(Case No. P043D2C3C)

In Re Application of:	)
FARMWALD et al.	)
	)
Serial No: 09/492,982	)
	)
Filed: JANUARY 27, 2000	)
	)
Title: METHOD OF OPERATING A MEMORY	)
DEVICE HAVING A VARIABLE DATA	)
INPUT LENGTH	)

Group
Art Unit: 2818

Before
Examiner: T. Nguyen

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to the Commissioner of Patents and Trademarks, Washington, D.C. 20231 on _April 26, 2001_

Neil Steinberg
(Name of Person Mailing Correspondence)

_____ 4-26-2001
Signature   Date

Assistant Commissioner for Patents
Washington, DC 20231

INFORMATION DISCLOSURE STATEMENT

Dear Sir:

In compliance with the duty of disclosure set forth in 37 C.F.R. §1.56, Applicants' submit concurrently herewith an Information Disclosure Statement (IDS) including modified Form PTO-1449.

Some of the documents listed in the PTO-1449 have been cited by a defendant in an action pending in U.S. District Court For Eastern District of Virginia case, namely in Rambus Inc. v. Infineon Technologies A.G., et al., as prior art against the inventions claimed in, among other patents, U.S. 6,034,918. The '918 patent is a parent of the instant application. Reference to these documents are listed on page 2 of the Defendents' AMENDED PRIOR ART NOTICE PURSUANT TO 35 U.S.C. §282 (hereinafter "PRIOR ART NOTICE"). A copy of the PRIOR ART NOTICE is enclosed herewith.

Furthermore, the construction or interpretation of a number of terms have recently been considered in a _Markman_ opinion issued in the above-mentioned litigation. A number of claims pending in the instant application incorporate or incorporated some of these terms including, for example, the terms "block size", "write request", and "bus". The term "write request" has been deleted from the pending claims (as

amended): The term "bus" has been deleted from some of the pending claims (as amended). A discussion of "block size" may be found on pages 41-47 of the *Markman* opinion, and a discussion of "bus" may be found on pages 17-41 of the *Markman* opinion.

By submission of this *Markman* opinion, Applicants make no statement as to the correctness of the constructions set forth therein. Indeed, as is apparent from that opinion, the court substantially adopted the constructions proposed by the defendants, and not that construction proposed by Rambus, the owner of the instant application. A copy of the *Markman* opinion is also enclosed herewith.

Respectfully submitted,

Date: April 26, 2001

Neil A. Steinberg
Reg. No. 34,735
650-947-5325

PTO-1449 (Modified)	ATTY. DOCKET NO. P043D2C3C	SERIAL NUMBER 09/492,982
U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	APPLICANT(S) FARMWALD ET AL.	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	FILING DATE JANUARY 27, 2000	GROUP ART UNIT 2818

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
TNT	4,755,937	July 5, 1989	Olier			
TNT	4,875,192	Oct 17, 1989	Matsumoto			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

TNT	Pelgrom et al., "A 32-kbit Variable-Length Shift Register for Digital Audio Application", IEEE Journal of Solid-State Circuits, vol. sc-22, no. 3, June 1987, pp 415-422
	Grover et al., "Precision Time-Transfer in Transport Networks Using Digital Crossconnect Systems", IEEE Paper 47.2 Globecom, 1988, pp 1544-1548
	Gustavson et al., "The Scalable Interface Project (Superbus)" (DRAFT), SCI-22 Aug 88-doc1 pp 1-16, August 22, 1988
	Knut Alnes, "SCI: A Proposal for SCI Operation", SCI-10Nov88-doc23, Norsk Data, Oslo, Norway, pp. 1-12, Nov. 10, 1988
	Knut Alnes, "SCI: A Proposal for SCI Operation", SCI-6Jan89-doc31, Norsk Data, Oslo, Norway, pp. 1-24, Jan 6, 1989
	Bakka et al., "SCI: Logical Level Proposals", SCI-6Jan89-doc32, Norsk Data, Oslo, Norway, pp. 1-20, Jan 6, 1989
	Knut Alnes, "Scalable Coherent Interface", SCI-Feb89-doc52, (To appear in Eurobus Conference Proceedings May 1989) pp. 1-8
	Boysel et al., "Four-Phase LSI Logic Offers New Approach to Computer Designer", Four-Phase Systems Inc. Cupertino, CA, Computer Design, April 1970, pp. 141-146,
TNT	Boysel et al., "Random Access MOS Memory Packs More Bits To The Chip", Electronics, Feb. 16, 1970, pp. 109-146,

EXAMINER TAN T. NGUYEN	DATE CONSIDERED 05/17/01

EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant.

PTO-1449 (modified)	ATTY. DOCKET NO. P043D2C3C	SERIAL NUMBER 09/492,982
U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	APPLICANT(S) FARMWALD ET AL.	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	FILING DATE JANUARY 27, 2000	GROUP ART UNIT 2818

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

T~T	Hansen et al., "A RISC MICROPROCESSOR WITH INTEGRAL MMU AND CACHE INTERFACE", MIPS Computer Systems, Sunnyvale, CA, IEEE 1986 pp 145-148
	Moussouris et al., "A CMOS PROCESSOR WITH INTEGRATED SYSTEMS FUNCTIONS", MIPS Computer Systems, Sunnyvale, CA, IEEE 1986 pp 126-130
	"LR2000 High Performance RISC Microprocessor Preliminary" LSI Logic Corp. 1988, pp. 1-15
	"LR2010 Floating Point Accelerator Preliminary" LSI Logic Corp. 1988, pp.1-20
	"High Speed CMOS Databook", Integrated Device Technology Inc. Santa Clara, CA, 1988 pp 9-1 to 9-14
	Riordan T. "MIPS R2000 Processor Interface 78-00005(C)", MIPS Computer Systems, Sunnyvale, CA, June 30, 1987, pp 1-83
T~T	Moussouris, J. "The Advanced Systems Outlook-Life Beyond RISC: The next 30 years in high-performance computing", Computer Letter, July 31, 1989 (an edited excerpt from an address at the fourth annual conference on the Advanced Systems Outlook, in San Francisco, CA (June 5))

EXAMINER Thu T. Nguyen	DATE CONSIDERED 05/17/01

EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant.

IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF VIRGINIA
(Richmond Division)

RAMBUS INC.,

Plaintiff-Counterclaim Defendant,

v.

INFINEON TECHNOLOGIES AG *et al.*,

Defendants-Counterclaim Plaintiffs.

Civil Action No. 3:00CV524

AMENDED PRIOR ART NOTICE PURSUANT TO 35 U.S.C. § 282

Defendants Infineon Technologies AG, Infineon Technologies North America Corp. and

Infineon Technologies Holding North America Inc. (collectively, "Infineon"), by their attorneys and

pursuant to 35 U.S.C. § 282, submit this amended prior art notice.

PATENTS

Inventor	Patent Number	Date
Nishiguchi	U.S. 4,445,204	April 24, 1984
Saccardi	U.S. 4,858,113	August 15, 1989
Kawai	U.S. 4,953,128	August 28, 1990
White	U.S. 5,140,688	August 18, 1992
Wiggers	U.S. 4,998,262	March 5, 1991
Grover	U.S. 5,361,277	November 1, 1994
Patel	U.S. 3,950,735	April 13, 1976
Wiener	U.S. 3,771,145	November 6, 1973
Redwine	U.S. 4,330,852	May 18, 1982

Inventor	Patent Number	Date
Bomba	U.S. 4,763,249	August 9, 1988
Glier	U.S. 4,755,937	July 5, 1988
Jackson	U.S. 4,315,308	February 9, 1982
Matsumoto	U.S. 4,875,192	October 17, 1989
James	U.S. 4,703,418	October 27, 1987
Horiguchi	U.S. 4,726,021	February 16, 1988
Kimoto	U.S. 4,870,562	September 26, 1989
Kawamasa	Japanese Patent Application 54-160587 / Sho 56-82961	July 7, 1981
Hasegawa	Japanese Patent Application 58-186919 / Sho 60-80193	May 8, 1985
Kumagai	Japanese Patent Application 62-185253 / Sho 64-29951	January 31, 1989
Taguri	Japanese Patent Application 55-89232 / Sho 57-14922	January 26, 1982
Yamaguchi	Japanese Patent Application 62-71428 / Sho 63-239676	October 5, 1988
Miyazaki	Japanese Patent Application Sho 60-55459	March 30, 1985
Hashimoto et al.	Japanese Patent Application S 61-72350	April 14, 1986
Petrich	U.S. 4,338,569	July 4, 1989
Chappell et. al.	U.S. 4,845,677	July 6, 1982

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PUBLICATIONS

Author(s)	Description	Date
Johnson et al.	A Variable Delay Line PLL for CPU-Coprocessor Synchronization. IEEE JSSC, Vol. 23, No. 5	October 1988
Pelgrom et al.	A 32 KBIT Variable Length Shift Register for Digital Audio Application, ESSCIRC, pp. 38-40	June 1986
Grover et al.	Precision Time-Transfer in Transport Networks Using Digital Crossconnect Systems, GLOBECOM (publication)	1988
Grover et al.	Precision Time-Transfer in Transport Networks Using Digital Crossconnect Systems, GLOBECOM (presentation)	1988
Pinkham et al.	A High Speed Dual Port Memory with Simultaneous Serial and Random Mode Access for Video Applications	December 1984
IBM	Fast Packet Bus for Microprocessor Systems with Caches, IBM TBD pp. 279-282	January 1989
Watanabe	Session XIX: High Density SRAMs, IEEE ISSCC, pp. 266-267	1987
Gustavson et al.	The Scalable Coherent Interface Project (Superbus), Draft	August 22, 1988
James	P1596: SCI, A Scalable Coherent Interface	November 28, 1988
James	Scalable I/O Architecture for Buses	November 28, 1988
Gustavson	Scalable Coherent Interface	November 28, 1988
Alnes	SCI: A Proposal For SCI Operation	November 10, 1988
Alnes	SCI: A Proposal For SCI Operation	January 6, 1989
Bakka et al.	SCI: Logical Level Proposals	January 6, 1989
Kristiansen	Scalable Coherent Interface	February 1989

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Author(s)	Description	Date
Kristiansen	Scalable Coherent Interface	September 1989
Boysel et. al	Random-Access MOS Memory Packs More Bits To The Chip	February 16,1970
Boysel et. al	Four-Phase LSI Logic Offers New Approach to Computer Designer	April 1970

OTHER PRIOR ART

Description	Date
Wiggers' Notes	March 1987 - January 1988
Siemens' SDA 9087 and SDA 9088 integrated circuits, described in "ICs For Entertainment Electronics – Picture-in-Picture System" (8/89)	1988-1989

KNOWLEDGEABLE PERSONS / PRIOR INVENTORS

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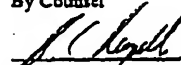
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Dated: March 9, 2001

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CERTIFICATE OF SERVICE
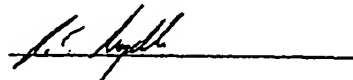
I certify that on this 9th day of March 2001, a copy of the foregoing AMENDED PRIOR ART NOTICE PURSUANT TO 35 U.S.C. § 282 was sent to Counsel for Rambus Inc. as listed below:

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IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF VIRGINIA
Richmond Division
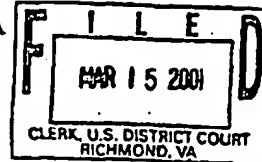
RAMBUS, INC.,

    Plaintiff,

v.   Civil Action No. 3:00cv524

INFINEON TECHNOLOGIES AG
and INFINEON TECHNOLOGIES
NORTH AMERICA CORP.,

    Defendants.

MEMORANDUM OPINION

This action involves four patents and fifty-seven claims. All four patents in suit descend from a common progenitor, the specification of which controls the patents in suit. The parties are in agreement that construction of the claims here at issue is confined to construction of eight disputed terms ("bus," "block size," "read request," "write request," "transaction request," "first external clock signal," "second external clock signal" and "integrated circuit device") each of which, with but one exception,[1] has the same meaning in each claim in issue in all four patents in suit. Hence, the agreed upon scope of claim construction is to construe the eight terms.

---

[1] The parties agree that all the terms have the same meaning throughout with the exception of "integrated circuit device." The Defendants contend that this term has a different meaning in one patent due to representations made to the Patent and Trademark Office during the prosecution of that patent.

The parties have briefed the issues, have presented evidence at a hearing conducted pursuant to the requirements of <u>Markman v.</u> <u>Westview Instruments, Inc.</u>, 517 U.S. 370 (1996), and have argued orally. Against this background, the eight disputed terms, and hence the claims, are accorded the constructions set forth below.

BACKGROUND

In 1990, the co-founders of Rambus, Inc. ("Rambus"), Mark Horowitz and Paul Michael Farmwald, filed a patent application describing numerous inventions designed to increase the operating speed of memory devices in computers. The Patent Office determined that this application, U.S. Patent App. No. 07/510,898 ("the '898 application"), actually contained 11 independent and distinct inventions, required Rambus to select only one of those inventions to pursue in the '898 application, and allowed Rambus to file divisional applications on the remaining inventions described in the '898 application. Rambus did precisely that, electing to pursue one invention within the '898 application and thereafter filing ten more applications in the next six months. Subsequently, continuation and divisional applications were filed on these ten applications; and thus, to date, Rambus has been granted 31 patents based on the 1990 '898 application. Numerous applications are currently pending.

By way of background, the patented inventions have to do with computer memory devices called Dynamic Random Access Memory

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("DRAM") and a system and devices for increasing the speed at which

data or information is transferred between the DRAM and the Central

Processing Unit ("CPU") of a computer. The DRAM is a high-speed,

short-term memory device where information being used by the CPU is

stored. The patents in suit describe numerous inventions

respecting the memory interface and a new type of "bus" which

carries information or data. The "Field of Invention" section of

the specification, common to all patents in suit, gives the

following overview of the inventions:

> [a]n integrated circuit bus interface for
> computer and video systems is described which
> allows high speed transfer of blocks of data,
> particularly to and from memory devices, with
> reduced power consumption and increased system
> reliability. A new method of physically
> implementing the bus architecture is also
> described.

U.S. Patent No. 6,034,918 (issued March 7, 2000) ("the '918

patent"), col. 1, ll. 20-25.[2]

On August 8, 2000, Rambus instituted this action for the

infringement of four of its patents against Infineon Technologies

AG (a German corporation), Infineon Technologies, Inc. (a German

corporation) Infineon Technologies North America Corp. (a Delaware

corporation) and Infineon Technologies Holding North America, Corp.

(a Delaware corporation) (collectively referred to as "Infineon").

---

[2] All the patents in suit, and all the patents springing from
the 1990 '898 application, contain the same specification. For
ease of citation, all references to the specification will be to
the '918 patent.

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The first of the patents in suit, U.S. Patent No. 5,953,263 (issued

Sept. 14, 1999) ("the '263 patent"), claims a latency invention

which involves the use of a programmable register on the DRAM chip

to store a value representative of a time delay. The latency

invention makes the DRAM response time more predictable because the

CPU knows precisely when it will receive data from the DRAM in

response to a transaction request, thereby allowing the system to

plan for transfers and improving overall traffic flow over the

bus.[3] Claims 1-5, 14, 16-19, 21, 23-25, 27-28, 30 and 32-33 of the

'263 patent are at issue in this action.

Secondly, in U.S. Patent No. 5,954,804 (issued Sept. 21, 1999)

("the '804 patent"), Rambus claims a delayed lock loop (DLL) on a

DRAM chip, which allows precise timing of the output of data. In

essence, the DLL allows the DRAM chip to collect the data from the

memory cells and then paces the release of that information over

the bus. The DLL becomes useful when operating the DRAM at high

---

[3]   Claim 1 of the '263 patent is representative of this
invention:

> 1. A synchronous semiconductor memory device
> having at least one memory section which
> includes a plurality of memory cells, the
> memory device comprises:
>
> a programmable register to store a value which
> is representative of a delay time after which
> the memory device responds to a read request.

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rates of speed.' Claim 26 of the '804 patent is the only claim involving this invention at issue in this action.

--- The third patent, U.S. Patent No. 6,034,918 (issued Mar. 7, 2000) ("the '918 patent"), covers the variable block size invention, which involves the use of circuitry to allow for the output of variable-sized blocks of data over the bus in response to a transaction request. The additional circuitry allows a user, such as a CPU, to select differing sizes or blocks of data, instead

---

' Claim 26 of the '804 patent describes DLL in combination with the latency invention:

> 26. An integrated circuit device having at least one memory section which includes a plurality of memory cells, wherein the integrated circuit device outputs data on an external bus synchronously with respect to first and second external clock signals, the integrated circuit device comprises:
>
> a first internal register to store a value which is representative of a number of clock cycles to transpire before the integrated circuit device responds to a read request;
>
> delay locked loop circuitry to generate an internal clock signal using the first and second external clock signals; and
>
> interface circuitry, coupled to the external bus to receive a read request, the interface circuitry includes a plurality of output drivers, coupled to the external bus, to output data on the external bus in response to the internal clock signal, synchronously with respect to the first and second external clock signals and in accordance with the value stored in the first internal register.

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of a single piece of data.[5] Claims 1-2, 6, 8-9, 13, 15-20, 24-25, 29-31, 33 and 34 of the '918 patent are at issue in this action.

Lastly, U.S. Patent No. 6,032,214 (issued Feb. 29, 2000) ("the '214 patent") claims double data rate ("DDR") as the invention. In general, memory devices send and receive information according to a clock contained within the computer system. Clocks are a common, but important, feature of all computer systems. Before the DDR invention, information was transferred only on the "tick" of the clock. The memory device using that type of transfer regulator is called a Synchronous DRAM, or "SDRAM." The DDR invention allows information from the SDRAM to be sent out on both the "tick" and

---

[5] Claim 18 of the '918 patent describes this invention as:

> 18. A method of operation of a synchronous memory device, wherein the memory device includes a plurality of memory cells, the method of operation of the memory device comprises:
>
> receiving an external clock signal;
>
> receiving first block size information from a bus controller, wherein the first block size information defines a first amount of data to be output by the memory device onto a bus in response to a read request;
>
> receiving a first request from the bus controller; and
>
> outputting the first amount of data corresponding to the first block size information, in response to the first read request, onto the bus synchronously with respect to the external clock signal.

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the "tock" (or the rising and falling edges) of the computer's internal clock, thereby doubling the data output of the SDRAM for a given clock rate.[6] Claims 1-2, 4, 6, 9-11, 14-16, 18-19, 21, 24-26 and 29 of the '214 patent are at issue in this action.

Infineon makes, uses, sells or offers to sell, and imports SDRAM devices, DDR SDRAM devices and Synchronous Graphics RAM ("SGRAM") devices, as well as products, such as computers, servers, automated teller machines, telephones and telephone systems and point of sale terminals, all of which contain SDRAM, DDR SDRAM or

---

[6] Claim 15 of the '214, which is representative of this invention, covers this invention in combination with the variable block size described in the '918 patent:

> A method of operation of a synchronous memory device, wherein the memory device includes a plurality of memory cells, the method comprising:
>
> receiving first block size information, wherein the first block size information defines a first amount of data to be output onto a bus in response to a read request;
>
> receiving a first read request; and
>
> outputting the first amount of data corresponding to the first block size information, in response to the first read request, onto the bus synchronously with respect to a first and a second external clock signal wherein a first portion of the first amount of data is output synchronously with respect to the first external clock signal and a second portion of the first amount of data is output synchronously with respect to the second external clock signal.

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SGRAM devices. Rambus alleges that all of those devices and the products and modules into which they are incorporated infringe some or all of the patents in suit. Infineon denies that its products infringe any of those patents.

DISCUSSION

I.   The Legal Standard

Patent infringement analysis involves two steps: ascertaining the proper construction of the patent claim and determining whether the accused method or product infringes the properly construed claim. Vitronics Corp. v. Conceptronic, Inc., 90 F.3d 1576, 1582 (Fed. Cir. 1996). A patent contains two distinct elements: "First, it contains a specification describing the invention 'in such full, clear, concise and exact terms as to enable any person skilled in the art . . . to make and use the same.' 35 U.S.C. § 112 . . . . Second, a patent includes one or more 'claims,' which 'particularly poin[t] out and distinctly clai[m] the subject matter which the applicant regards as his invention." Markman v. Westview Instr., Inc., 517 U.S. 370, 373 (1996).

The construction or interpretation of a claim is a question of law. Markman v. Westview, 52 F.3d 967, 979 (Fed. Cir. 1995) (en banc), aff'd 517 U.S. 370 (1996). "[I]n interpreting an asserted claim, the court should look first to the intrinsic evidence of record, i.e., the patent itself, including the claims, the

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specification and, if in evidence, the prosecution history. Such intrinsic evidence is the most significant source of the legally operative meaning of disputed claim language." Vitronics, 90 F.3d at 1582 (internal citations omitted). If the intrinsic evidence is insufficient to resolve ambiguity in the meaning of claims, the court may rely upon extrinsic evidence to understand the technology and to construe the claims. Id. at 1584. "Extrinsic evidence is that evidence which is external to the patent and file history, such as expert testimony, inventor testimony, dictionaries, and technical treatises and articles." Id. Extrinsic evidence, however, may not be used to contradict the claim language or the meanings established in the specification. Id. "Any other rule would be unfair to competitors who must be able to rely on the patent documents themselves, without consideration of expert opinion that then does not even exist, in ascertaining the scope of a patentee's right to exclude." Id. (quoting Southwall Tech. Inc. v. Cardinal IG Co., 54 F.3d 1570, 1578 (Fed. Cir. 1995), cert. denied, 516 U.S. 987 (1995)).

In the examination of the intrinsic evidence, "there is a hierarchy of analytical tools. The actual words of the claim are the controlling focus." Digital Biometrics, Inc. v. Identix, Inc., 149 F.3d 1335, 1344 (Fed. Cir. 1998). Thus, a court should first "look to the words of the claims themselves, both asserted and nonasserted, to define the scope of the patented invention."

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Vitronics, 90 F.3d at 1582. See Pitney Bowes, Inc. v. Hewlett-Packard Co., 182 F.3d 1298, 1305 (Fed. Cir. 1999) ("The starting point for any claim construction must be the claims themselves."); K-2 Corp. v. Salomon S. A., 191 F.3d 1356, 1362 (Fed. Cir. 1999) ("We begin, of course, with the language of the claims").

"The general rule is that terms in the claim are to be given their ordinary and accustomed meaning." Id. See also Vitronics, 90 F.3d at 1582. "It is the person of ordinary skill in the field of the invention through whose eyes the claims are construed. Such person is deemed to read the words used in the patent documents with an understanding of their meaning in the field, and to have knowledge of any special meaning and usage in the field." Multiform Desiccants, Inc v. Medzam. Ltd., 133 F.3d 1473, 1477 (Fed. Cir. 1998). Notwithstanding that terms in the claim and specification are presumed to carry the ordinary meaning that they would have to one of ordinary skill in the field, "a patentee may choose to be his own lexicographer and use terms in a manner other than their ordinary meaning, as long as the special definition of the term is clearly stated in the patent specification or file history." Vitronics, 90 F.3d at 1582. See also Hoescht Celanese Corp. v. BP Chems. Ltd., 78 F.3d 1575, 1578 (Fed. Cir. 1996), cert. denied 519 U.S. 911 (1996) ("A technical term used in a patent document is interpreted as having the meaning that it would be given by persons experienced in the field of the invention, unless

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it is apparent from the patent and the prosecution history that the inventor used the term with a different meaning").

> That is, the ordinary and accustomed meaning of a disputed claim term is presumed to be the correct one, subject to the following. First, a different meaning clearly and deliberately set forth in the intrinsic materials -- the written description or the prosecution history -- will control. Second, if the ordinary and accustomed meaning of a disputed term would deprive the claim of clarity, then further reference must be made to the intrinsic -- or in some cases, extrinsic -- evidence to ascertain the proper meaning. In either case, a party wishing to alter the meaning of a clear claim term must overcome the presumption that the ordinary and accustomed meaning is the proper one, demonstrating why such an alteration is required.

K-2 Corp., 191 F.3d at 1362-63 (internal citations omitted). See Hoganas AB v. Dresser Indus., Inc., 9 F.3d 948, 951 (Fed. Cir. 1993) ("Although a patentee can be his own lexicographer, as we have repeatedly said, the words of a claim will be given their ordinary meaning, unless it appears that the inventor used them differently." (internal quotations omitted)). Cf. Johnson Worldwide Assoc., Inc. v. Zebco Corp., 175 F.3d 985, 990 (Fed. Cir. 1999) (indicating that the patentee must set "forth an explicit definition for a claim term"). "Thus, second, it is always necessary to review the specification to determine whether the inventor has used any terms in a manner inconsistent with their ordinary meaning." Vitronics, 90 F.3d at 1582 (emphasis added); CVI/Beta Ventures, Inc. v. Tura LP, 112 F.3d 1146, 1153 (Fed. Cir.

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1997), cert. denied 522 U.S. 1109 (1998) (same). See also Toro Co.

v. White Consolidated Indus., Inc., 199 F.3d 1295, 1299 (Fed. Cir.

1999) ("words of ordinary usage must nonetheless be construed in

the context of the patent documents").

> The specification acts as a dictionary when it expressly defines terms used in the claims or when it defines terms by implication. . . . The specification contains a written description of the invention which must be clear and complete enough to enable those of ordinary skill in the art to make and use it. Thus, the specification is always highly relevant to the claim construction analysis. Usually, it is dispositive; it is the single best guide to the meaning of a disputed term.

Vitronics, 90 F.3d at 1582 (emphasis added). The ordinary meaning

of claim terms is a "heavy presumption" to be overcome. Johnson

Worldwide, 175 F.3d at 989.

As the third category of intrinsic evidence, "the court may

also consider the prosecution history of the patent, if in

evidence. This history contains the complete record of all the

proceedings before the Patent and Trademark Office ["PTO"],

including any express representations made by the applicant

regarding the scope of the claims." Vitronics, 90 F.3d at 1583

(internal citations omitted). "[A]rguments made during prosecution

regarding the meaning of a claim term are relevant to the

interpretation of that term in every claim of the patent absent

some clear indication to the contrary." Southwall Tech., 54 F.3d

at 1579. "The prosecution history limits the interpretation of

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claim terms so as to exclude any interpretation that was disclaimed during prosecution." Id. at 1576. "Claims cannot be construed in one way to obtain their allowance and in a different way against accused infringers." Id. See Digital Biometrics, 149 F.3d at 1344 ("The prosecution history is relevant because it may contain contemporaneous exchanges between the patent applicant and the PTO about what the claims mean").

When consideration of these three sources resolves the disputes over the asserted claim terms (as it generally should), reliance on extrinsic evidence to construe the claim is improper. Vitronics, 90 F.3d at 1583. This is because the claims, specification and file history comprise the public record of the patentee's claim, and to allow the public record (upon which competitors are entitled to rely when investigating the scope of the patentee's claimed invention), to be altered or changed by extrinsic evidence is to undermine the notice function of the public record. Id.

The preference for intrinsic evidence, however, does not preclude a court from considering or relying upon extrinsic evidence:

> Vitronics does not prohibit courts from
> examining extrinsic evidence, even when the
> patent document is itself clear. . . .
> Moreover, Vitronics does not set forth any
> rules regarding the admissibility of expert
> testimony into evidence. . . . Rather,
> Vitronics merely warned courts not to rely on
> extrinsic evidence in claim construction to

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> contradict the meaning of claims discernible
> from thoughtful examination of the claims, the
> written description, and the prosecution
> history--the intrinsic evidence.

Pitney Bowes, 182 F.3d at 1308 (emphasis in original). See also

Bell & Howell Document Mngmt. Prods. Co. v. Altek Sys., 132 F.3d

701, 706 (Fed. Cir. 1997) ("Use of expert testimony to explain an

invention may be useful. But reliance on extrinsic evidence to

interpret claims is proper only when the claim language remains

genuinely ambiguous after consideration of the intrinsic evidence.

. . .").

> This is especially the case with respect to
> technical terms, as opposed to non-technical
> terms in general usage or terms of art in the
> claim-drafting art. . . . Indeed, a patent is
> both a technical and a legal document. While
> a judge is well-equipped to interpret the
> legal aspects of the document, he or she must
> also interpret the technical aspects of the
> document, and indeed its overall meaning, from
> the vantage point of one skilled in the art.

Pitney Bowes, 182 F.3d at 1309.

Within the category of extrinsic evidence, some types of

evidence are preferred over others: "prior art documents and

dictionaries, . . . are more objective and reliable guides [than

expert testimony]. Unlike expert testimony, these sources are

accessible to the public in advance of litigation. . . . Indeed,

opinion testimony on claim construction should be treated with the

utmost caution, for it is no better than opinion testimony on the

meaning of statutory terms." Id. at 1585.

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These fundamental precepts inform and guide the construction of the claims at issue in this action. As mentioned previously, there are 57 different claims being asserted under the four patents in suit and each of those claims are in dispute and therefore must be construed. However, in their claim construction briefs the parties have circumscribed that rather daunting task by identifying eight terms to be interpreted. At the _Markman_ hearing, the parties agreed that (with a previously noted exception) these eight terms have the same meaning in each of the 57 asserted claims. As a result, the claim construction task in this action reduces to construing the eight disputed terms. That task is undertaken _seriatim_.

II. Claim Construction

A. "Bus"

The parties dispute the meaning of "bus" as that term is used throughout the claims of the patents in suit. Rambus argues that "bus" means any "set of signal lines (for example, wires) to which a number of devices are connected, and over which information is transferred between devices." According to Rambus, "the term "bus" is old and very common in the electrical arts" and, in the patents in suit, the term is used in its ordinary and customary sense "as a set of signal lines over which information is transferred."[7] To

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[7] Plaintiff Rambus Inc.'s _Markman_ Brief Concerning Claim Construction, p. 13.

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support the contention that this is the ordinary and customary construction of the term "bus," as used in its patents, Rambus relies not upon intrinsic evidence but upon the extrinsic evidence of the *IEEE (Institute of Electrical and Electronics Engineers) Standard Dictionary of Electrical and Electronics Terms,* Fourth Ed., IEEE Inc., New York (1988), p. 116, to explain how one skilled in the art would understand the term. The IEEE Dictionary defines a bus as "a set of signal lines used by an interface system, to which a number of devices are connected, over which information is transferred between the devices." Id.[*]

Infineon, on the other hand, contends that "bus" actually has a specialized meaning conferred by the specification of the patents in suit, which describes and explains the bus and its use with the other inventions as the Rambus "multiplexed bus." Before the '898 application was filed in 1990, most buses generally had point-to-point interfaces wherein the CPU would communicate with different memory devices by different and separate lines. Furthermore, within each bus in the prior art, the lines would be dedicated to

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[*] Of course, a court cannot use an inconsistent dictionary definition to contradict the meaning derived from the intrinsic evidence, but such definition may be of some assistance to the court in interpreting technical terms. See Vanguard Prods. Corp. v. Parker Hannifin Corp., 234 F.3d 1370, 1372 (Fed. Cir. 2001) ("Although a dictionary definition may not enlarge the scope of a term when the specification and the prosecution history show that the inventor, or recognized usage in the field of the invention, have given the term a limited or specialized meaning, a dictionary is often useful to aid the court in determining the correct meaning to be ascribed to a term as it was used.")

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carrying either data, address, control or device-select information. In the new inventive Rambus bus, a single bus is multiplexed so that the bus lines carry all the address, control, data and device-select information over a single bus. In Infineon's view, the use of the term "bus" throughout the claims is limited to the new inventive bus described in the specification.

1. The Claim Language

The analysis begins by first considering the claim language.[9] Most of the 57 claims at issue use the term "a bus" or "the bus" or "an external bus." None of the claims, however, expressly define the term "bus," nor do they dispositively support either proposed definition. Rather, the claims generally speak of outputting or inputting data over a bus.

Infineon urges the court to consider the language of claim 26 of the '918 patent as illustrative of its view of the term

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[9] The term "bus" is used in claims 1, 2, 6, 8, 16, 18, 19, 20, 24, 33, and 14 of the '918 patent, claims 1, 2, 4, 10, 15, 16, 18, and 25 of the '214 patent, claims 2, 14, 27, and 30 of the '263 patent and claim 26 of the '804 patent.

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26. An integrated circuit device having at least one memory section which includes a plurality of memory cells, wherein the integrated circuit device _outputs data on an external bus_ synchronously with respect to first and second external clock signals, the integrated circuit device comprises:

. . .

interface circuitry, _coupled to the external bus to receive a read request_, the interface circuitry includes a plurality of output drivers, coupled to the external bus, to output data on the external bus in response to the internal clock signal, synchronously with respect to the first and second external clock signals and in accordance with the value stored in the first internal register.

'918 patent, Claim 26 (emphasis added). Infineon posits that this claim calls for data to be output onto the bus, and a read request to be received on the _same bus_, thus supporting its conclusion that "bus" means a multiplexed bus.[10] While the language of this single claim somewhat supports Infineon's construction, the specification must reviewed to determine how the inventors used the term "bus" and whether they intended the term to have a special meaning. See Watts v. XL Sys., Inc., 232 F.3d 877, 882 (Fed. Cir. 2000) ("One purpose for examining the specification is to determine if the patentee has limited the scope of the claims"). "[E]ven if [the claims] were clear on their face, [the court] must consult the

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[10] The testimony of Infineon's expert, Mr. Joseph McAlexander also supports this conclusion. See Markman Hearing, Tr. pg. 370 1. 13 to pg. 371, 1. 19 (explaining that claim 1 of the '918 patent clearly indicates that a read request and output data are to travel across a single bus).

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specification to determine if the patentee redefined any of those terms." Id. at 883.

2. The Specification

A close study of the patent specification reveals that, not only did the inventors act as their own lexicographers in defining the term "bus" to be the new inventive bus, but they also repeatedly explained how their various inventions worked in conjunction with the new bus, which they describe to be a centerpiece of the systems they claim to have invented.

The specification clearly and unambiguously describes the bus of the invention to be the inventive multiplexed bus. In the "Summary of Invention" the specification states:

> The present invention includes a memory subsystem comprising at least two semiconductor devices, including at least one memory device, connected in parallel to a bus where the bus includes a plurality of bus lines for carrying substantially all address, data and control information needed by said memory devices, where the control information includes device-select information and the bus has substantially fewer bus lines than the number of bits in a single address, and the bus carries device-select information without the need for separate device-select lines connected directly to individual devices.

'918 patent, col. 3, ll. 50-60 (emphasis added). And again, later in the same section, the specification states, "In this system of this invention, DRAMs and other devices receive address and control information over the bus and transmit or receive requested data

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<u>over the same bus.</u> Each memory device contains only a single bus interface with no other signal pins." '918 patent, col. 4, lines 9-13 (emphasis added). <u>See also</u> '918 patent col. 3, l. 61 through col. 4 l. 1. (the DRAM "is modified to use a wholly bus-based interface rather than the prior art combination of point-of-point and bus-based wiring used with conventional versions of these devices. The new bus includes clock signals, power and multiplexed address, data and control signals").

Throughout the "Detailed Description," the specification repeatedly explains the use of the new multiplexed bus:

> The present invention is designed to provide <u>a high speed, multiplexed bus</u> for communication between processing devices and memory devices and to provide devices adapted for use in the bus system.
>
> ∗ ∗ ∗
>
> The bus consists of a relatively small number of lines connected in parallel to each device on the bus. The bus carries substantially all address, data and control information needed by devices for communication with other devices on the bus. In many systems using the present invention, <u>the bus carries almost every signal between every device in the entire system. There is no need for separate device-select lines since device-select information for each device on the bus is carried over the bus. There is no need for separate address and data lines because address and data information can be sent over the same lines.</u>
>
> ∗ ∗ ∗
>
> Virtually all the signals needed by the computer system can be sent over the bus.

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'918 patent, col. 5, ll. 29-45 (emphasis added). The inescapable lesson that emerges from comparing the claims of the patents with the inventors' fulsome textual description of the invention is that the inventions include a new bus and new devices that work with the inventive bus, all to the inventor's stated purpose, which is "_to provide_ a _high speed multiplexed bus_ for communication between processing devices and memory devices _and to provide devices adapted for use in the bus system._" '918 Patent, col. 5, ll. 29-33 (emphasis added).

Additionally, not only does the specification define "bus" to be a multiplexed bus, but it also sets a background for explaining how the inventive multiplexed bus works with various other features of Rambus' inventions. Thus, the explanation of the inventions also supports the conclusion that the term "bus" means the multiplexed bus. For example, every embodiment described in the specification involves the use of a multiplexed bus.[11] Not once do

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[11] _See e.g._ '918 patent, col. 4, ll. 1-4 ("In a preferred implementation, 8 bus data lines and an AddressValid bus line carry _address, data and control information_ for memory addresses up to 40 bits wide.") (emphasis added); '918 patent, col. 5, ll. 59-64 ("In the preferred implementation, memory devices are provided that have _no connections other than the bus connections described herein_ and CPUs are provided that use _the bus of this invention_ as the principal, if not exclusive, connection to memory and to other devices on the bus.") (emphasis added); '918 patent, col. 8 ll. 17-25 ("The preferred bus architecture of this invention comprises 11 signals: BusData[0:7]; AddrValid; Clk1 and Clk2; plus an input reference level and power and ground lines connected in parallel to each device . . . . The bus lines for BusData[0:7] signals form a byte-wide, multiplexed data/address/control bus").

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the patents indicate that any of the inventions can, or should be, used with the prior art dedicated bus architecture.

This understanding is confirmed by the testimony of Mr. Joseph McAlexander, Infineon's expert, who explains that the patents "describe several bus architectures. But in every instance when they describe the bus of the invention it is always a multiplexed address, data and control bus." Markman Hearing, Tr. p. 360, l. 25 to p. 361, l. 4. Rambus' expert did not refute this conclusion.

In Toro Co. v. White Consolidated Indus., Inc., 199 F.3d 1295 (Fed. Cir. 1999), the Federal Circuit found it significant that the disputed patent contained only one embodiment of the invention. On the issue of whether a "ring" described in the patent must be attached to the "cover," the court noted that:

> The specification and drawings show the restriction ring as 'part of' and permanently attached to the cover. No other structure is illustrated or described. . . .
>
> . . . This is not simply the preferred embodiment; it is the only embodiment. . . .
>
> . . . Nowhere in the specification, including its twenty-one drawings, is the cover shown without the restriction ring attached to it.

Id. at 1301. See also O.I. Corp. v. Tekmar Co. Inc., 115 F.3d 1576, 1581 (Fed. Cir. 1997) (rejecting patentee's argument that the invention could have smooth or cylindrical walls when "[a]ll of the 'passage' structures contemplated by the written description are thus either non-smooth or conical."); General Amer. Transp. Corp.

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v. Cryo-Tran, Inc., 93 F.3d 766, 770 (Fed. Cir. 1996), cert. denied 520 U.S. 1155 (1997) (the disputed claim construction was "not just the preferred embodiment of the invention; it is the only one described. Nothing in the claim language, specification, or drawings suggests that any of the [limitations] may be eliminated . . .") (emphasis in original). Likewise, it is significant here that Rambus does not list a single example of how any of the new inventions would work with any type of bus other than a multiplexed bus.[12]

The Federal Circuit's holding in Wang Labs., Inc. v. America Online, Inc., 197 F.3d 1377 (Fed. Cir. 1999) is instructive as well. In Wang, the court considered whether the ordinary and

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[12] The failure of the specification to describe any other kind of bus in connection with the invention distinguishes the principal decision upon which Rambus relies, Johnson Worldwide Assoc., Inc. v. Zebco Corp., 173 F.3d 985 (Fed. Cir. 1999). In Johnson Worldwide, the Federal Circuit placed great emphasis upon the fact that the disputed claims did not require the narrower construction. 175 F.3d at 991. The Johnson Worldwide opinion distinguished Laitram Corp. v. Morehouse Indus., Inc., 143 F.3d 1456 (Fed. Cir. 1998) (which adopted the narrower claim construction) because the written description in Laitram made clear that the asserted claims will bear only one interpretation. In Johnson Worldwide, there was no such unambiguous language in the claim; "nothing suggests that 'heading' is required to be the heading of a trolling motor." Johnson Worldwide, 175 F.3d at 991.

The facts of Johnson Worldwide are distinguishable from the Rambus patents here. The Johnson Worldwide court noted that the "many uses of the term throughout the . . . patent are consistent with a broader definition" and that the "[v]aried use of the term in the written description demonstrates the breadth of the term rather than providing a limited definition." Id. at 991. Thus, the dual usage of the term did not create "a special and particular definition" Id. Here, there are not varied uses of the term "bus," only a single multiplexed bus.

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accustomed meaning of the term "frame" could be overridden by the
inventor's explanation in the specification:

> The parties agreed before the district court
> that the term "frame" can in general usage be
> applied to bit-mapped display systems as well
> as to character-based systems . . . . The
> disagreement was as to whether the term
> "frame" in the '669 claims embraced this
> general usage, or whether the term would be
> understood by persons of skill in this field
> as limited to the character-based systems
> described in the '669 patent.

Wang, 197 F.3d at 1381. As is true here, the only system described

and enabled in the specification and drawings in Wang used the

narrower, specific arrangement of the character-based system. Id.

at 1382. The only time that the patent mentioned non-character-

based systems was in the "Background of Invention" section. Id.

The Federal Circuit agreed with the district court's conclusion

that those references were merely acknowledgments of the state of

the prior art, not an enlargement of the patent's invention; and

that a person skilled in the field of art would not have understood

that those references were included in the applicant's invention.

Id. Similarly, Rambus is limited to the description set forth in

the specification, which is only a description of the multiplexed

bus.

In an effort to distance the claims from the specification,

Rambus argues that one skilled in the art would recognize that any

kind of bus could be used with the many inventions of the

specification, not just the new multiplexed bus. The Federal

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Circuit has rejected this exact argument, which attempts to escape
the language of the specification. See Watts, 232 F.3d at 883
(inventor's arguments that "one of ordinary skill would be aware of
a myriad ways to effect a sealing connection . . . may be true,
[but] it does not overcome the fact that the specification
specifies that the invention uses misaligned taper angles"). The
fact that the inventions might conceivably be used with any kind of
bus does not overcome the oft-repeated assertions in the
specification which describe, and even tout, the new Rambus
inventive bus while demonstrating that the inventions are to be
used with the multiplexed bus.

Rambus next argues that Infineon is trying to improperly limit
the scope of the claim to the limitations described in the
preferred embodiment. See Karlin Tech., Inc. v. Surgical Dynamics,
Inc., 177 F.3d 968, 973 (Fed. Cir. 1999) ("The general rule, of
course, is that the claims of a patent are not limited to the
preferred embodiment, unless by their own language."); CVI/Beta
Ventures, 112 F.3d at 1158 ("as a general matter, the claims of a
patent are not limited by preferred embodiments"). The
specification, however, clearly distinguishes between the
"invention" of the multiplexed bus and "the preferred embodiment"
of the bus. The patent often describes the broader invention of a
bus multiplexed for address, data and control information. This
description is then followed by a narrower description of the

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'preferred embodiment' that is an implementation of the multiplexed

bus.

For example, the patent states:

> The new bus includes clock signals, power and
> multiplexed address, data and control signals.
> In a preferred implementation, 8 bus data
> lines and an AddressValid bus line carry
> address, data and control information for
> memory addresses up to 40 bits wide. Persons
> skilled in the art will recognize that 16 bus
> data lines or other numbers of bus data lines
> can be used to implement the teaching of the
> invention.

'918 patent, col. 3, l. 67 through col. 4, l. 7. (emphasis added).

The new multiplexed bus is the broadly defined invention and the

preferred embodiment has certain characteristics such as 8 or 16

mutliplexed lines, an AddressValid line, and addresses of up to 40

bits. Numerous references in the specification highlight these

differences.[13] Usually, the preferred embodiments described in the

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[13] See e.g. 918 patent, col. 5, ll. 37-50 ("The bus carries
substantially all address, data, and control information needed by
devices for communication with other devices on the bus. . . .
Using the organization described herein, very large addresses (40
bits in the preferred implementation) and large data blocks (1024
bytes) can be sent over a small number of bus lines 8 plus one
control line in the preferred implementation)."); '918 patent col.
14, ll. 49-67 ("In the bus-based system of this invention" a master
can use the device ID to access a specific device "including the
address and control registers. In the preferred embodiment, one
master is assigned to carry out the entire system configuration
process." (emphasis added); '918 patent, col. 16., ll. 12-21 ("The
bus architecture of this invention can include more than one master
device. The reset or initialization sequence should also include
a determination of whether there are multiple masters on the bus,
and if so to assign unique master ID numbers to each. Persons
skilled in the art will recognize that there are many ways of doing
this. For instance, the master could poll each device to determine

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specification give a technical example of how the overall invention

works, thus helping to explain the claim language. "Although

claims are not necessarily restricted in scope to what is shown in

a preferred embodiment, neither are the specifics of the preferred

embodiment irrelevant to the correct meaning of claim limitations."

Phonometrics, Inc. v. Northern Telecom, Inc., 133 F.3d 1459, 1466

(Fed. Cir. 1998). Where, as here, the several embodiments

described in the specification each involves only a multiplexed

bus, that weighs heavily in construing the term bus to mean a

multiplexed bus. See Wang, 197 F.3d at 1383.

Finally, it is significant that the specification only

mentions the generic (or "dedicated") bus architecture in the

"Comparison of Prior Art" section.[14] In these references to "bus,"

however, the inventors are distinguishing their new inventive bus

from the prior art. The inventors explain that "[n]one of the

buses described in patents or other literature use only bused

connections. All contain some point-to-point connections on the

backplane." '918 Patent, col. 2, l. 67 to col. 3, l. 3. Thus, it

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what kind of device it is . . . .") (emphasis added).

[14] For example, the specification explains that the bus of an
earlier patent (U.S. Patent No. 3,821,715) "multiplexes addresses
and data over a 4-bit wide bus and uses point-to-point control
signals to select particular RAMs or ROMs." '918 patent, col. 2 ll.
13-15. The specification also explains that in the DRAM of a
previous patent (U.S. Patent 4,449,207) "[t]he external interface
to this DRAM is convention, with separate control, address and data
connections." '919 patent, col. 2, ll. 32-33.

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does not help Rambus to point out, as it does, that this text of the comparison uses the same term ("bus") to describe a completely different architecture from the "new" bus which, according to Rambus, means that the term "bus" must necessarily encompass any set of information transfer lines, including those cited as prior art. The "Comparison With Prior Art" section states only what the invention does not cover; and, in so doing, the specification expressly distinguishes the prior art buses from the disclosed bus of the invention. Of course, it is settled that "[c]laims are not correctly construed to cover what was expressly disclaimed." Culter Corp. v. A.E. Staley Mfg. Co., 224 F.3d 1328, 1331 (Fed. Cir. 2000) (description in specification that distinguished other types of catalysts "effected a disclaimer of the other prior art acids"). See also Wang, 197 F.3d at 1382 (references to "bit-mapped" protocols in "Background of Invention" were acknowledgments of the state of the art and not an enlargement of the invention described in the patent). The argument which Rambus makes based on the term "bus" as used in the discussion of prior art runs afoul of this basic precept of claim construction.

In a further effort to use the discussions of prior art to support its proposed definition of "bus," Rambus relies on Clearstream Wastewater Sys. v. Hydro-Action, Inc., 206 F.3d 1440 (Fed. Cir. 2000), to argue that its inventions involve "combination

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claims," therefore it is entirely permissible to include both the new and the generic buses in its inventions:

> In construing the disputed claim limitations, it must be kept in mind that the claims at issue in this case are combination claims. Combination claims can consist of new combinations of old elements or combinations of new and old elements. Because old elements are part of these combination claims, claim limitations may, and often do, read on prior art.

Id. at 1445 (internal citations omitted). Further, Clearstream explains that:

> Clearly, the written description does point out the disadvantages of the [prior art] rigid conduit system and the advantages of the [new] flexible-hose system. However, the written description does not require that only the new flexible-hose system, but not the old, rigid conduit system, could be used in the claimed wastewater treatment plant. It is well established in patent law that a claim may consist of all old elements . . . for it may be that the combination of old elements is novel and patentable. Similarly, it is well established that a claim may consist of all old elements and one new element, thereby being patentable.

Id. (emphasis added).

Infineon properly agrees that combination claims can include some, or even all, prior art elements. However, Infineon also is correct in asserting that the proper framework for the current analysis is whether one of ordinary skill in the art would understand the Rambus disclosure to assert the combination theory recently embraced by Rambus. The patent specification here does

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not support that theory because, unlike _Clearstream_, the specification in Rambus' patents do not describe the generic prior art bus in combination with any of the claims. Indeed, the "Comparison With Prior Art" discussion is at considerable pain to dissociate the inventive bus, and its uses, from the prior art, and to establish a similar disconnect of the other inventions from the prior art. '918 Patent, col. 2, l. 7 to col. 3, l. 47.

Thus, the specification clearly demonstrates that when the inventors used the term "bus" in the claims, they were referring to the new multiplexed bus described in the specification.[15] Upon reading the patent, one skilled in the art would conclude that the patentee explicitly defined bus: "[t]he present invention includes a memory subsystem comprising at least two semiconductor devices . . . . connected in parallel to a bus where the bus includes a plurality of bus lines for carrying substantially all address, data and control information needed by said memory devices." '918 patent, col. 3, ll. 50-55. Nothing in the specification - no drawing and no embodiment - indicates that the bus in the claims has the dictionary definition that Rambus now asserts.

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[15] Other than the "Comparison with Prior Art" section, the patent specification only once indicates that a bus can be anything but the multiplexed bus: "Persons skilled in the art recognize that certain devices, such as CPUs, may be connected to other signals lines and possibly to independent buses, for example a bus to an independent cache memory, in addition to the bus of this invention." '918 patent, col. 5, ll. 54-57. In this reference, the inventors clearly distinguish between the multiplexed bus of the invention and any other kind of bus to be used in the system.

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3. The File History

Despite the obvious descriptions in, and implications of, the patent itself, Rambus argues that the patent history teaches that the term "bus" includes more than just the multiplexed bus. While it is doubtful that a court should look to the patent history to contradict the unambiguous meaning described in the specification, see Multiform Desiccants, 133 F.3d at 1478 ("[w]hen the specification explains and defines a term used in the claims, without ambiguity or incompleteness, there is no need to search further for the meaning of the term"), the patent history here does not in any fashion clarify the scope of the disputed term. Rambus relies upon two statements made, and actions taken, in the prosecution of the patents stemming from the 1990 '898 application.

In June 1997, during the prosecution of the parent application[16] to the '263 patent (which is also the grandparent to the '918 patent),[17] the Patent Examiner issued a requirement for

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[16] This application eventually issued as U.S. Patent No. 5,841,580.

[17] When considering a patent's prosecution history, it is proper to look to statements made in the prosecution of related patents stemming from the same application, as is the case here. See Elkay Mfg. Co. v. Ebco Mfg. Co., 192 F.3d 973, 980 (Fed. Cir. 1999) ("When multiple patents derive from the same initial application, the prosecution history regarding a claim limitation in any patent that has issued applies with equal force to subsequently issued patents that contain the same claim limitation."); Mark I Marketing Corp. v. R.R. Donnelley & Sons Co., 66 F.3d 285, 291 (Fed. Cir. 1995) ("Thus, the relevant prosecution history here includes not only the '659 application but also the parent '815 and grandparent '668 applications."); Jonsson v.

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restriction under 35 U.S.C. § 121,[18] finding that this patent
claimed two distinct inventions. The examiner divided the claims
into two groups, one group describing a plurality of conductors to
be used with the multiplexed bus and the second group describing an
access-time register within the memory device (the latency
invention).[19] Asserting that the groups were not "connected in

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Stanley Works, 903 F.2d 812, 818 (Fed. Cir. 1990) (prosecution
history of parent application is relevant to understanding scope of
claims issuing in a continuation-in-part application).

[18] A requirement for restriction is issued by the PTO when a
patent application contains more than one distinctly claimed
invention. 35 U.S.C. § 121.

[19] The June 9, 1997 Office Action explains:

> 4. Restriction to one of the following
> inventions is required under 35 U.S.C. 121:
>
> Group I. Claims 151-55, drawn to a
> memory device having a plurality of conductors
> being multiplexed for sequentially receiving
> an address, classified in Class 365, subclass
> 230.02.
> Group II. Claims 156-158, drawn to a
> semiconductor device having at least one
> access-time register, classified in Class 395,
> subclass 290.
> The inventions are distinct, each from
> the other because of the following reasons:
>
> 5. Inventions I and II are disclosed as
> different combinations which are not connected
> in design, operation or effect. These
> combinations are independent if it can be
> shown that (1) they are not disclosed as
> capable of use together, (2) they have
> different modes of operation, (3) they have
> different functions, or (4) they have
> different effects. (MPEP 806.04, MPEP
> 808.01). In the instant case the combinations

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design, operation, or effect," the Patent Examiner required the inventors to elect to pursue only one group of claims. Rambus prosecuted the claims in Group II (the latency invention), resulting in the '580 patent.

From this action by the PTO and from the fact that the same Patent Examiner reviewed the '263 and '918 patents in suit, Rambus asks the Court to make the leap in logic that the PTO must have understood that the multiplexed bus was not necessary for every other invention arising from the specification. This kind of speculation into the motivations of the patent examiner is not useful to a reviewing court or a competitor reading the patent history. "It is the <u>applicant's</u> representations during the prosecution that potentially shed light on the construction of the claims." <u>Laitram Corp. v. Morehouse Indus., Inc.</u>, 143 F.3d 1456, 1462-63 (Fed. Cir. 1998) (emphasis in original) (rejecting argument

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[sic] the memory device in Group I does not require the access-time register of Group II, and the semiconductor device in Group II does not require the plurality of conductor being multiplexed to receive an address as claimed in Group I.

6. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, and the search required for invention I is not required for invention II, restriction for examination purposes as indicated is proper.

(emphasis added).

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that meaning could be derived from the representation of the reexamination requester). The snippet of patent history upon which Rambus relies only shows that: (a) a single Patent Examiner at one time indicated that some claims should not be lumped together, and (b) that, rather than making an affirmative response to this restriction, Rambus chose to drop the claims for the multiplexed bus and pursue the latency invention. No more can be inferred from this exchange.

Rambus also relies on a second piece of evidence contained in the file history. Specifically, in November 1995, a different Patent Examiner rejected claims pending in the grandparent to the '804 patent as being obvious in view of prior art reference, U.S. Patent No. 5,129,069 to Helm, et al. Under Rambus' view of the file history, the Patent Examiner must have equated the generic term "bus" (recited in claims 176-181 of the grandparent application) with the non-multiplexed bus contained in the Helm patent when he initially rejected the claims. Nevertheless, this same Patent Examiner allowed claim 26 of the '804 patent (which contains a reference to an external bus) to issue without requiring that the term "bus" be limited to a multiplexed bus. Again, this kind of guessing as to what a Patent Examiner may have been thinking is not generally helpful to construing the claim terms because it requires both the court and the public to pour over oftentimes complex and voluminous patent histories, speculate as to

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the motivation behind an office action, and then follow the patents
in an effort to divine whether that same Patent Examiner may have
had reason to construe another claim in the same manner. This
invitation to haphazard guesswork certainly cannot be considered
sufficiently reliable to trump the clear language of the
specification. See Vitronics, 90 F.3d at 1582 ("Usually, [the
specification] is dispositive; it is the single best guide to the
meaning of a disputed term").

Moreover, the standard for construing claims in the patent
application process is far different than the standard for
construing claims in a litigation context. Patent examiners
construe claims under a broader standard than that used by a court
in undertaking claim construction. The Federal Circuit has held
that "[i]t would be inconsistent with the role assigned to the PTO
in issuing a patent to require it to interpret claims in the same
manner as judges who, post-issuance, operate under the assumption
that the patent is valid." In re Morris, 127 F.3d 1048, 1054 (Fed.
Cir. 1997). In the posture of a claim construction during
litigation, if the intrinsic evidence is ambiguous, "another claim
construction canon comes into play. Because the applicant has the
burden to 'particularly point[] out and distinctly claim[] the
subject matter which the applicant regards as his invention' 35
U.S.C. § 112, ¶ 2 (1994), if the claim is susceptible to a broader
and a narrower meaning, and the narrower one is clearly supported

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by the intrinsic evidence while the broader one raises questions of enablement under § 112, ¶ 1, we will adopt the narrower of the two." Digital Biometrics, 149 F.3d at 1344. See also Athletic Alternatives, Inc. v. Prince Mfg. Inc., 73 F.3d 1573, 1581 (Fed. Cir. 1996) ("Were we to allow AAI successfully to assert the broader of the two senses of 'between' against Prince, we would undermine the fair notice function of the requirement that the patentee distinctly claim the subject matter disclosed in the patent from which he can exclude others temporarily.") Therefore, even if one were to conclude that the patent history casts doubt on the clear meaning of the specification (which it does not), Rambus should be limited to the embodiment and description of a multiplexed bus set forth in the specification because it is the narrower of the two constructions.

The simple fact here is that reference to the file history does not contradict the clarity given by the specification. What Rambus has done is fixate upon two isolated events in the file history and, without connecting them to the issued patents, urges the Court to ascribe significance to the events by divining what an examiner must have meant by directing a certain action. That kind of sophistry is not among the tools available for claim construction under the carefully defined protocol established for that task by the Federal Circuit.

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4. Claim Differentiation

Rambus relies on the doctrine of claim differentiation to support its contention that "bus" means only a "generic" bus. The doctrine presumes "a difference in meaning and scope when different words or phrases are used in separate claims. To the extent that the absence of such difference in meaning and scope would make a claim superfluous, the doctrine of claim differentiation states the presumption that the difference between claims is significant." Toro Co., 199 F.3d at 1302 (Fed. Cir. 1999) (quoting Tandon Corp. v. United States Int'l Trade Comm'n, 831 F.2d 1017, 1023 (Fed. Cir. 1987)). Rambus highlights the claims contained in Rambus U.S. Patent No. 5,983,320 (the '320 patent),[20] in which the independent claims of the '320 patent cover the concept of the "new" multiplexed bus. Each claim contains qualifying language to limit the bus to one that carries multiplexed address, data and control information over the same bus. For example, claim 7 of that patent claims a method for programming memory having a bus, where the bus "compris[es] a group of general purpose signal lines carrying substantially all of the time-division multiplexed address, data and control information for a memory transaction, wherein the

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[20] The '320 patent is a "sister" or "brother" patent to the '804 patent. Rambus bases the notion of cross-patent claim differentiation on footnote 2 of Laitram Corp. v. Morehouse Indus., Inc., 143 F.3d 1456, 1460 n.2 (1998). Because the argument of claim differentiation fails for other reasons, it is assumed, without deciding, that this is a proper use of related patents and their prosecutions.

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address information is indicative of a range of addresses for a corresponding one of the individually addressable discrete memory sections of the memory device . . . ."[21] Therefore, Rambus argues that, when it wanted to limit the term "bus" to a bus that carries multiplexed information, it knew how to do so.

This argument is unavailing because it too contradicts the clear meaning of the specification. "The doctrine of claim differentiation cannot broaden claims beyond the scope that is supported by the specification." ATD Corp. v . Lydall, Inc., 159 F.3d 534, 541 (Fed. Cir. 1998). See also Multiform Desiccants, 133 F.3d at 1480 (same). "Although the doctrine of claim differentiation may at times be controlling, construction of claims is not based solely upon the language of other claims; the doctrine cannot alter a definition that is otherwise clear from the claim language, description, and prosecution history." O.I. Corp. v. Tekmar Co., Inc., 115 F.3d 1576, 1582 (Fed. Cir. 1997) (concluding "that the description provides a clear meaning for the language of the claim in this case and that it trumps the doctrine of claim differentiation"). See Toro Co., 199 F.3d at 1302 (claim differentiation "does not override clear statements of scope in the

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[21] According to Rambus, other Rambus patents include similar limiting language: U.S. Patent No. 5,995,443, Claim 33 ("the bus further includes a plurality of conductors terminated by an impedance to a power source") and U.S. Patent No. 6,032,215, Claims 33 and 37 (same) and Claim 38 ("the bus further includes a plurality of conductors wherein each conductor is terminated at an end by a resistor to a power terminal.")

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specification and the prosecution history"). "The presumption that separate claims have different scope 'is a guide, not a rigid rule.'" ATD Corp., 159 F.3d at 541 (quoting Autogiro Co. of Am. v. United States, 384 F.2d 391, 404 (1967)). Having determined that the written specification limits the term "bus" to a multiplexed bus, it would be impermissible to allow Rambus to rely upon claim differentiation (citing to other patents) to broaden the meaning of the term.[22]

5. The Extrinsic Evidence

A review of the intrinsic evidence clearly demonstrates that when the term "bus" is used in the claims, it means the new inventive Rambus multiplexed bus. "Because the intrinsic record is

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[22] Along these same lines, Rambus argues that the claims of the original '898 application specifically claim a multiplexed bus, therefore the reasoning behind claim differentiation would apply to give "bus" a generic meaning within the specification because the original claims are part of the specification. See In re Dossel, 115 F.3d 942, 945 (Fed. Cir. 1997) ("The statute thus makes clear that under current law the specification of a patent consists of, and contains, both a written description of the invention and the claims."); Northern Telecom, Inc. v. Datapoint Corp., 908 F.2d 931, 938 (Fed. Cir. 1990) ("The original claims as filed are part of the patent specification.") However, Dossel explains that "[m]odern usage . . . does not always conform to that statutory structure. For example, when discussing the process of claim construction, it is not uncommon for the process to be described as requiring an examination of the claims, the specification, and the prosecution history, treating them as distinct entities." 115 F.3d at 945. To the extent that the claims of the original application (which never issued), indicates that the inventors distinguished between the new multiplexed bus and a generic bus, this difference does not trump the clear descriptions in and implications of the written description.

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clear, (the court) do(es) not give weight to an inconsistent dictionary definition," <u>Digital Biometrics</u>, 149 F.3d at 1346, as offered by Rambus.

A reading of the entire specification, without parsing it into individual quotes, unmistakably conveys that one of the primary benefits of every invention claimed in the patents in suit, and described in the specification, is to increase the speed of operation of the memory device. High speed access is the crown jewel of the specification and to that end, the multiplexed bus, in combination with the other inventions, increases the transfer speeds and decreases the amount of space occupied by the transfer lines. One skilled in the art reading the specification would certainly conclude that the "bus" meant to be used with the inventions is the new, inventive, high-speed, multiplexed bus. This conclusion is supported by the testimony of Joseph McAlexander, an expert who is experienced in the art and whose explanation for reaching that conclusion is highly credible because it is fully consonant with the specification and the claim language as explicated by the specification.[23] Mr. McAlexander's testimony

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[23] <u>See</u> Markman Hearing, Tr. p. 379, l. 20 to p. 380, l. 3 (Mr. McAlexander states, "Because the patent very strongly distinguishes numerous times the multiplex bus of the invention from the prior art, and states specifically in numbers of places, that the bus architecture of this new bus design is essential for the type of high speed activity that is required across the bus, and it distinguishes from the prior art because the prior art is stated not to be able to give that high speed type of transaction.")

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is consistent with, and complimentary of, the intrinsic evidence.[24]

On the other hand, the testimony of Rambus' expert, Dr. William Huber, is at odds with the intrinsic evidence and depends on a dictionary definition (other extrinsic evidence) that is not consistent with the many descriptions given by the inventors in the specification.

6. Construction

For the foregoing reasons, the term "bus" means a multiplexed set of signal lines used to transmit address, data and control information.

B. "Block Size Information"

In Rambus' invention, the user can specify the amount of data to be transferred over the bus during a bus transaction. This value is represented by the term "block size." The parties differ as to exactly how this value is to be measured. Rambus argues that "block size" is "the number of sequential data bits to be read from or written to the memory." In essence, Rambus reads block size to be a function of the number of sequential transactions on a bus necessary to respond to the transaction request. Infineon posits that "block size" "specifies the total amount of data that is to be

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[24] Other portions of Mr. McAlexander's testimony generally support this construction. See Markman Hearing, Tr., pg. 361, 11. 14-24; pg. 364, 1. 22 to pg. 365, 1.22; pg. 367, 1. 17 to pg. 368, 1. 13; pg. 371, 11. 3-19.

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transferred on the bus in response to a transaction request." In

other words, Infineon measures block size as a function of size or

the amount of data to be transferred over the bus.

1.   The Claim Language

The term "block size" occurs numerous times throughout the

claims of the '918 patent and the '214 patent.[25] Most of the claims

indicate that block size information defines the amount of data to

be output or input by the memory device.[26] Indeed, there is nothing

in the text of any claim which employs the term "block size" to

indicate that "block size" means anything other than the amount of

data to be transferred on the bus in response to some sort of

transaction request.   Thus, from reading the language of the

claims, one skilled in the art would conclude that block size

information is an instruction indicating the amount of data to be

output (or input) by the memory device.

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[25] See claims 1, 2, 6, 9, 13, 15, 16, 18, 19, 20, 24, 29, 30, 31, 33, and 34 of the '918 patent and claims 1, 4, 6, 9, 10, 15, 16, 18, 21 and 25 of the '214 patent.

[26] See e.g. '918 patent, claim 1 ("first block size information defines a first amount of data to be output by the memory device. . . ."); '918 patent, claim 6 ("the memory device outputs the first amount of data corresponding to the first block size information. . . ."; '918 patent claim 13 ("the first block size information is a binary representation of the amount of data to be output after receipt of the first read request."); '214 patent, claim 1 ("first block size information defines a first amount of data to be output onto a bus. . . ."); '214 patent, claim 6 ("first block size information is a binary code indicative of the first amount of data to be output in response to the read request").

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Rambus nonetheless urges that block size means "the number of sequential data bits to be read from or written to the memory" (presumably in response to a transaction request) Rambus does not identify any aspect of the claim language that would support its preferred definition. Additionally, it is worth noting that nothing in the claim language has been cited, or for that matter argued, as supporting the temporal or order requirements which would inhere in a sequential-based definition.

2. The Specification

In general terms, the specification explains that "[o]ne object of the present invention is to use a new bus interface built into semiconductor devices to support high-speed access to <u>large blocks of data</u> from a single memory device by an external user of the data, such as a microprocessor, in an efficient and cost-effective manner." '918 patent, col. 3, lines 21-25 (emphasis added). <u>See also</u> '918 patent, col. 4, lines 15-16 ("The bus supports large data block transfers . . .").

In discussing the preferred method of Device Address Mapping and the address registers therein employed, the specification explains that:

> The address registers can include a single pointer, usually pointing to a <u>block of known size</u>, a pointer and a fixed or variable <u>block size value</u> or two pointers, one pointing to the beginning and one to the end (or to the "top" and "bottom" of each memory block.

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'918 Patent, col. 7, 11. 36-41. This text and that which follows
it clearly bespeaks volume or amount as the measure of a block, not
sequence or time.

The several other references to block size in the
specification also teach that the term relates to _amount_ of data
not the order and timing of bits of data in a particular sequence.[27]

3. The Extrinsic Evidence

The construction offered by Rambus purports to be grounded in
a table in column 11 of the specification. The table is in a
section which refers to the preferred embodiment detailed in Figure
4 of the patent.[28] The specification states:

> BlockSize[0:3] specifies the size of the data
> block transfer. If BlockSize[0] is 0, the
> remaining bits are the binary representation
> of the block size (0-7). If BlockSize[0] is
> 1, then the remaining bits give the block size
> as a binary power of 2, from 8 to 1024. A
> zero-length block can be interpreted as a
> special command, for example, to refresh a
> DRAM without returning any data, or to change
> the DRAM from page mode to normal access mode
> or vice-versa.

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[27] '918 Patent, col. 11, 11. 1-5, 11. 41-48; col. 16, 11. 26-
35, 11. 44-47; col. 17, 11. 1-2; col. 20, 11. 18-22.

[28] Figure 4 is replicated later in the Memorandum Opinion at
II.C.2.

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Block Size[0:2]	Number of Bytes in Block
0-7	0-7 respectively
6	8
9	16
10	32
11	64
12	128
13	256
14	512
15	1024

Persons skilled in the art will recognize that
other block size encoding schemes or values
can be used.

'918 patent, col. 11, ll. 41-63.[29]

Rambus uses Table 11, as interpreted by its expert, Dr. Huber,

as the basis for its construction that block size information is

the number of sequential transfers necessary to carry the desired

information over the bus line. The table is but one of many

encoding schemes and does not purport to define or explain the

meaning of block size generally. According to Dr. Huber, the block

size indicated in the chart corresponds to the number of sequential

transfers necessary to output the data onto the preferred

embodiment 8-line bus. That is certainly not apparent from the

patent document. Furthermore, during the Markman hearing, Dr.

Huber connected almost all of his opinions, not to the patent

specification, but rather to a prepared animation demonstrating how

block size should be measured as sequential transfers of data. The

reason for such reliance seems quite clear -- there simply is no

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[29] During the Markman hearing, the parties agreed that the "6"
contained in the second row of the chart is incorrect due to an
apparent copying error. This number should be an "8."

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support in the patent document. Also, that view is flatly contradicted by Infineon's expert who explained that block size contains information specifying the total amount of data that is to be transferred. See Markman Hearing, Tr. pg. 442, 11. 11-19. Mr. McAlexander has testified that "[t]he person of ordinary skill in the art would come to [the conclusion] that block size . . . means amount, and in just a plain, simple ordinary meaning of size is a[n] amount, it's not when or how." Markman Hearing, Tr. pg. 439, 11. 11-16 (testimony of Mr. McAlexander).

4. Construction

Infineon's construction is grounded in the specification and the claim language because both sources of information rather clearly reflect that block size is an amount of data, not the order in which it is delivered. There is nothing in the specification to support Rambus' somewhat contorted definition of block size. It simply defies reason (and the specification) to conceive of size as a measure of time.

Moreover, the construction urged by Rambus utterly ignores the clear language of the claim that block size is associated with a transaction request. (See, e.g., '918 Patent, Claim 1-7 and all other claims (8 through 38) dependent upon Claim 1-7). Infineon's definition encompasses this connection and, for that additional reason, it is the definition that is necessitated by the claim language and by the specification. Thus, "block size" is construed

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to mean "information that specifies the total amount of data that is to be transferred on the bus in response to a transaction request."

    C.   "Read Request," "Write Request," and "Transaction Request"

The next three disputed terms are closely related, and, as the parties agree, it is appropriate to accord joint consideration. The purpose of memory devices (i.e., a DRAM) is to store data for later use. To this end, when a controller (or master) accesses the memory device to either store or retrieve data, it must send that device an instruction indicating what type of transaction is to be performed. At the most basic level, a read request is an instruction to the memory device to read data from the memory cells; a write request instructs the memory device to write data to the memory cells; and a transaction request instructs the memory device to perform some function, which could include reading or writing data. The controversy surrounding these terms involves whether these requests must contain not only the instruction of what action to perform (found in an "AccessType" field), but also must include address information indicating where in the memory cells the data should be read or written. Rambus contends that read, write and transaction requests contain only the instruction of what action to perform. For example, it proposes that read request be defined as "an instruction to read data from specified

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memory cell(s) of the memory. This instruction is specified by a binary code[30] provided to the memory device during a single clock cycle and received by the memory device in response to a clock transition."

Infineon, on the other hand, argues that such requests must contain both the instruction of what kind of action to perform and address information indicating where that action is to occur on the memory device. Address information, containing both row and column identifiers, tells the memory device where the desired data is located (or to be located) within the plurality of the memory cells. In Infineon's construction, a "'read request' means 'a series of bits transmitted over the bus that contain multiplexed address and control information needed to request a read of data from a memory device.'" In addition to objecting to the failure of Rambus' definition to include address information, Infineon disagrees with the limitations inherent in Rambus' definition, specifically the requirements that the request be a "binary code," that it can be no longer than "a single clock cycle" of information, and that it must be "received in response to a clock transition." In its view, these limitations are not required by

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[30] Binary code, a term not in dispute here, is "a code that makes use of members of an alphabet containing exactly two characters, usually 0 and 1." *IEEE Standard Dictionary of Electrical and Electronics Terms*, 4th Ed., IEEE, Inc. NY, 4th Ed. Pg. 95.

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the intrinsic evidence, and in some cases are actually inconsistent with the embodiments disclosed in the specification.

1. The Claim Language

Both parties agree that the terms "read request," "write request," and "transaction requests" are not terms of art and were used for the first time in the 1990 '898 application. Therefore, there is no ordinary and accustomed meaning for these terms. Some information, however, can be gleaned from the language of the claims.[31]

Infineon uses the language of claim 1 of the '918 patent, claim 1 of the '214 patent, claim 1 of the '263 patent and claim 26 of the '804 patent to demonstrate that all claims require that a device respond to 'read request':

> 1. A method of controlling a synchronous memory device, wherein the memory device includes a plurality of memory cells, the method of controlling the memory device comprises:
>
> providing first block size information to the memory device, wherein the first block size information defines a first amount of data to

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[31] The term "read request" occurs in claims 1, 6, 8, 13, 18, 19 24, 29, and 34 of the '918 patent; claims 1, 2, 6, 14, 15, 16, 18, and 29 of the '214 patent; claims 1, 2, 14, 24, 15, 27, and 30 of the '263 patent; and claim 26 of the '804 patent.
The term "write request" occurs in claims 2 and 20 of the '918 patent.
The term "transaction request" occurs in claims 18 and 25 of the '263 patent.

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be output by the memory device onto a bus in
response to a read request . . .

'918 patent, claim 1 (emphasis added).

1. A method of operating a synchronous memory
device, wherein the memory device includes a
plurality of memory cells, the method
comprising:

providing first block size information to the
memory device, wherein the first block size
information defines a first amount of data to
be output onto a bus in response to a read
request . . .

'214 patent, claim 1 (emphasis added).

1. A synchronous semiconductor memory device
having at least one memory section which
includes a plurality of memory cells, the
memory device comprises:

a programmable register to store a value which
is representative of a delay time after which
the memory device responds to a read request.

'263 patent, claim 1 (emphasis added).

26. An integrated circuit device having at
least one memory section which includes a
plurality of memory cells, wherein the
integrated circuit device outputs data on an
external bus synchronously with respect to
first and second external clock signals, the
integrated circuit device comprises:

a first internal register to store a value
which is representative of a number of clock
cycles to transpire before the integrated
circuit device responds to a read request. . .

'804 patent, claim 26 (emphasis added).

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The claims clearly so provide. Indeed, all but two of the disputed claims containing these terms[32] explicitly state that information is supplied "in response to" a read request, a write request or other transaction request. It is, of course, true, as Infineon contends, that, in order to "respond" to a request (i.e. outputting or inputting data), the desired response can only occur if the selected device is given the information necessary to generate that response. Because one of ordinary skill in the art would understand that both address and control information are required for the memory device to respond to a request, that request must contain more than just the binary code or "AccessType" suggested by Rambus. Given the nature of the information and the way the invention works, it seems self-evident from the claim language that a request is, as Infineon posits, a series of bits transmitted over the bus containing address and control information. This conclusion is further buttressed by the explanations of Mr. McAlexander. See Markman Hearing, Tr. pg. 417, 11. 18-25 ("certainly the read has to have some control. It tells you what kind of transaction is being requested. If the memory is to respond to that, it must know where to respond from, what

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[32] Indeed, of those claims mentioning read request, write request and transaction request, only claims 14 and 29 of the '214 patent do not explicitly mention that the memory device is to respond to the read request and even those mention a read request in such a way as to indicate that the term means there what it means elsewhere (Claim 14 "before executing another read request"); (Claim 29 "after executing another read request.")

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The claims clearly so provide. Indeed, all but two of the disputed claims containing these terms[32] explicitly state that information is supplied "in response to" a read request, a write request or other transaction request. It is, of course, true, as Infineon contends, that, in order to "respond" to a request (i.e. outputting or inputting data), the desired response can only occur if the selected device is given the information necessary to generate that response. Because one of ordinary skill in the art would understand that both address and control information are required for the memory device to respond to a request, that request must contain more than just the binary code or "AccessType" suggested by Rambus. Given the nature of the information and the way the invention works, it seems self-evident from the claim language that a request is, as Infineon posits, a series of bits transmitted over the bus containing address and control information. This conclusion is further buttressed by the explanations of Mr. McAlexander. See Markman Hearing, Tr. pg. 417, 11. 18-25 ("certainly the read has to have some control. It tells you what kind of transaction is being requested. If the memory is to respond to that, it must know where to respond from, what

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address"). Thus, the claim language, although not dispositive, strongly supports the view of read, write and transaction request taken by Infineon.

2. The Specification

Although not discussed as extensively as other terms, such as "bus," the terms here at issue are the subject of explication in the specification. For example, in the "Comparison With Prior Art" section, the inventors explain:

> Yet another <u>object of this invention</u> is to provide <u>a method</u> for <u>transferring address, data and control information</u> over a relatively narrow bus and to provide a method of bus arbitration when multiple devices seek to use the bus simultaneously.

'918 Patent, col. 3, 11. 35-39 (emphasis added). This statement of object remarks the key role of address, data and control information. And, as explained in the cited text, and above in construing the term "bus," the significance of the invention of the system is to accomplish quickly the commands necessary to initiate a request and secure a response.

Then, in the ensuing "Summary of Invention" discussion, the inventors say that "[i]n this system of the invention, <u>DRAMs and other devices receive address and control information</u> over the bus and <u>transmit or receive requested data</u> over the same bus." '918 Patent, col. 4, 11. 9-11 (emphasis added). Though not explicitly mentioning a "request," this quote lends credence to the basic

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notion that a memory device should receive both address and control information in order to be able to transmit or receive data.

Then, shortly thereafter, in describing a preferred implementation of the invention, the specification explains how a bus transaction is initiated "by sending a request packet (a sequence of bytes comprising address and control information)." '918 Patent, col. 6, 11. 60-63). This, too, teaches that a request (be it a read request, write request, or transaction request) includes the address and control information necessary to accomplish the request.[33]

Having established that the specification contemplates both address and control information are needed for a response, it is necessary to ascertain whether a read request should contain <u>both</u> categories of information. The definition which Rambus presses proposes that a transaction request would consist only of the "AccessType" found in the top row[34] of Figure 4, the preferred embodiment.

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[33] Again, this conclusion is supported by the expert testimony of Infineon's Mr. McAlexander. See Trans. pg. 417, lines 20-22 ("I found the control and address information were required in every instance that it was addressed in the specification").

[34] As shown in Figure 4, the rows represent time or clock cycles.

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REGULAR ACCESS

ADDRVALID	BUSDATA[0:7]	24	CYCLE
1	ACCESSTYPE[0:3] : MASTER[0:3]		0 - EVEN
	ADDRESS[0:8]	25	1 - ODD
	ADDRESS[9:17]		2
	ADDRESS[18:26]		3
	ADDRESS[27:35]	26	4
0	ADDRESS[36:39] : BLOCKSIZE[0:3]		5

(left-margin reference numbers: 23, 22, 27; lower-right reference: 23)
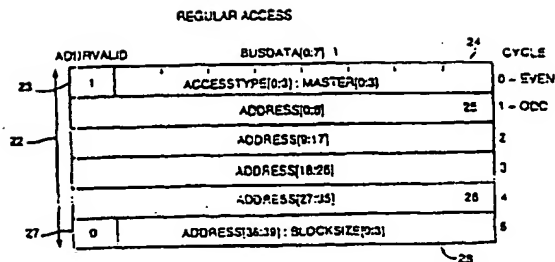
FIG_4

In the preferred embodiment, the AccessType instruction, which
contains the control information specifying the type of request,
would be a binary code 4-bits wide. The specification explains:

> The AccessType filed [sic: field] specifies
> whether the requested operation is a read or
> write . . . . In a preferred implementation,
> AccessType[0] is a Read/Write switch: if it is
> a 1, then the operation calls for a read from
> the slave (the slave to read the requested
> memory block and drive the memory contents
> onto the bus); if it is a 0, the operation
> calls for a write into the slave (the slave to
> read data from the bus and write it to
> memory).

'918 patent, col. 9, ll. 47-56. Rambus would limit the terms "read
request," "write request" and transaction request" to only this
AccessType field.   In contrast, according to Infineon's
interpretation, the requests must contain both the AccessType
control information and the address information indicated on the
remaining rows of Figure 4. To support its definition, Infineon
points to the following passage from the specification:

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In a preferred implementation of the invention, to initiate a bus transfer over the bus, a master sends out a request packet, a contiguous series of bytes containing address and control information . . . .

The device-selection function is handled using the bus data lines. AddrValid is driven, which instructs all slaves to decode the request packet address, determine whether they contain the requested address, and if they do, provide the data back to the master (in the case of a read request) or accept data from the master (in the case of a write request) in a data block transfer.

'918 patent, col. 8 l. 66 through col. 9, l. 4. The specification also explains that "[i]n some cases, a slave [memory device] may not be able to respond correctly to a request, e.g. for a read or write. In that situation, the slave should return an error message . . . . or a retry message." '918 patent, col. 12, ll. 4-8. These references and others[35] illustrate that the memory should <u>respond</u> to the request. In order to respond, the memory device also must be given address information specifying where the data is to be read or written.

Additionally, though one must understand the technology to comprehend the import of the statement, the specification actually states that address rows are to be accessed during a request. The patent explains that the DRAM sense amps should be pre-charged and

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[35] <u>See</u> e.g. '918 patent, col. 8, ll. 48-49 ("a slave should preferable respond to a request in a specified time"); '918 patent, col. 8, ll. 24-29 ("AddrValid is used to indicate when the bus is holding a valid address request, and instructs a slave to decode the bus data as an address and, if the address is included on that slave, to handle the pending request."

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"[t]his precharging allows access to a <u>row</u> in the RAM to begin as soon as the access request for either <u>inputs (writes) or outputs (reads)</u> is received and allows the column sense amps to sense data quickly." '918 Patent, col. 10, 11. 21-24 (emphasis added). Because one skilled in the art would recognize that "row" refers to a particular location on the plurality of memory cells, it follows that address information must be conveyed in order to access that row. That address information is contained in "the access request for either inputs (writes) or outputs (reads)."

Rambus definition would only indicate what type of operation to take place. <u>See</u> Markman Hearing, Tr. pg. 122, 11. 11-13 (testimony of Dr. Huber) ("We don't need the rest of the information [address information] to know that it's a read request"). The specification and the claims, however, clearly demonstrate the memory devices are not only to recognize the requested operation, but also respond to the request. Even Dr. Huber admitted that address information must be received for there to be a response. Dr. Huber took the view that this information could be conveyed at some other unspecified time. <u>See</u> Markman Hearing, Tr. pg. 141, 11. 20-22 (testimony of Dr. Huber). That approach is untenable because nowhere in the specification is it mentioned that address information should be sent at any other time than contemporaneous with the request.

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Nor does the specification support the other foundational components of the narrow view of these terms expressed by Rambus. The construction urged by Rambus essentially attempts to equate the term "read request" with "AccessType," as shown in Figure 4, as the predicate for its requirement that "a read request" must be a binary code, occur in a single clock cycle, and be in response to a clock transition. The specification offers no warrant for such a limited construction, and, as Infineon points out, Rambus here is attempting artificially to limit the invention to the preferred embodiment of Figure 4, which describes a bus transaction that uses the preferred implementation of a 9-bit wide external bus. See '918 patent, col. 9, 11. 26-27 ("Each request packet uses all nine bits of the multiplexed data/address lines"). Because Figure 4 indicates that the AccessType is only 4-bits wide, it is possible for Rambus' proposed definition to occur in a single clock cycle. However, this requirement stems solely from Rambus' view that AccessType is a request. If a request contains both control and address information, then this would not be true. See Markman Hearing, Tr. pg. 431, 11. 8-12 (testimony of McAlexander) ("There is a specific control set of bits called the access type that does occur as a set of bits in a particular single cycle as shown in a preferred embodiment, but all that does is establish the type.") Similarly, there is nothing in the specification to support Rambus' requirement that the transaction request be received by the memory

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device in response to a clock transition. See Markman Hearing, Tr. pg. 432, ll. 2-9 (testimony of McAlexander) (indicating that nothing in the specification supports this requirement).

Rambus contends that Infineon's construction incorrectly equates "read request" (or "write request" or "transaction request") with a request packet, arguing instead that a read request is actually a component of a request packet. For example, the specification states that "FIG. 4 shows the format of a request packet." '918 patent, col. 4, l. 66. It also explains that, in a preferred implementation, "a master sends out a request packet, a contiguous series of bytes containing address and control information." '918 patent, col. 8, ll. 60-63. The criticism is superficially appealing; however, the confusion results in large part from the fact that the specification uses the term "request" and "request packet" interchangeably. For example, the inventors explain, "FIG. 5 illustrates the format of a retry message 28 which is useful for read requests, . . . All DRAMs and masters can easily recognize such packet as an invalid request packet, and therefore a retry message." '918 patent, col. 12, ll. 33-39. See also '918 patent, col. 12, ll. 49-52 ("The master sends request packets and keeps track of periods when the bus will be busy in response to that packet. The master can schedule multiple requests so that the corresponding data block transfers do not overlap."; '918 patent, col. 12, ll. 58-61 ("Situations will arise, however,

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where two or more masters send a <u>request packet</u> at or about the same time and the multiple <u>requests</u> must be detected. . . .) That drafting lapse is unfortunate, but it certainly is not dispositive because that text too must be interpreted in perspective of the whole specification.

Considering the claim language and the specification in its entirety and for the reasons explained above, the construction offered by Infineon is better supported by the patent document. Although that construction results in some overlap in the meanings of request and request packet, that overlap is inherent in the patent specification itself. Indeed, the most significant passage of the specification discussing read requests and write requests indicates that such a request is related to (if not synonymous with) a request packet: "AddrValid is driven, which instructs all slaves to decode the <u>packet</u> address determine whether they contain the requested address, and if they do, provide the data back to the master (in the case of <u>read request</u>) or accept data from the master (in the case of a <u>write request</u>) in a data block transfer." '918 Patent, col. 8, l. 66 through col. 9, l. 4 (emphasis added).

3.   The File History

Those constructions derived from the claim language and specification are supported by the fact that, in the prosecution of the '804 patent, Rambus made statements to the PTO relating to the term "transaction request." In February 1999, Rambus submitted a

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Preliminary Amendment in U.S. Patent App. 08/798,525 (issued as the '804 patent) in which it admitted that transaction requests are not simply a single clock-cycle access-time code. In response to a rejection by the Patent Examiner, Rambus stated that a "transaction request" contains identification information:

> When the identification information <u>contained in the transaction request</u> corresponds to the identification value stored in the internal register in a particular memory device on the module, that memory device <u>executes the transaction request</u>. Memory devices on the module having identification values which do not correspond to the <u>identification information contained in the transaction request</u> do not execute or respond to the request.

Supplemental Preliminary Amendment, U. S. Patent App. 08/798,525, p. 12 (emphasis added). Thus, Rambus explicitly represented that a transaction request contains more than just a binary code in the AccessType field: the above passage shows that device identification information also is contained in the transaction request. While this representation does not necessarily imply that Infineon's definition is unquestionably correct, it certainly undermines the construction now urged by Rambus.

4.   Claim Differentiation

Claim 15 of the '214 patent refers to a "read request" without further limitation, while dependent claim 22 recites: "The method of claim 15 wherein the first block size information and the first read request are contained in a request packet." Rambus argues

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that this language distinguishes a "read request" from a "request packet." As stated previously, the specification sometimes uses the terms "request" and a "request packet" interchangeably. Notwithstanding that drafting laxity, the differences in claim 15 and 22 do not refute the notion that a request contains address and control information. These claims simply add a third type of information, block size information, as a component of a request packet.

Given that the claim language clearly illustrates that a memory device is to respond to a read, write or transaction request and that Rambus has not explained how the device would respond without receiving address, data and control information, the claim language on its face supports the requirement that requests contain both address and control information. The specification, while not pellucid, also indicates that a request must contain such information so that it can respond to the request, whether the request be packetized or not. Rambus' narrow definition is not supported by the specification, and indeed, is refuted by the file history. Therefore, it is appropriate to conclude that "read request," "write request," and "transaction request" contain both address and control information indicating what type of transaction to perform and where the data should be located on the memory device.

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5. Construction

For the foregoing reasons, the term "read request" is construed to mean "a series of bits transmitted over the bus that contain multiplexed address and control information needed to request a read of data from a memory device." The term "write request" is construed to mean "a series of bits transmitted over the bus that contain multiplexed address and control information needed to request a write of data to a memory device." The term "transaction request" is construed to mean "a series of bits transmitted over the bus that contain multiplexed address and control information needed to perform a transaction over the bus with a memory device."

D. "First and Second External Clock Signals"

The parties agree that the bus of the invention carries two external clock signals[36] which pace the exchange of information over the bus and provide timing synchronization for the memory system. The dispute arises over whether the second external clock signal must contain information that is different from the timing information sent by the first clock signal.

Although referred to as a "clock" by one skilled in the art, the clock of a memory chip is actually a set of timing information

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[36] As has been the convention of both the patent documents and the parties, the terms "clock signal" and "clock" are used interchangeably.

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derived from an oscillating reference voltage ("V_{REF}") which cycles between two voltage levels. Rambus' proposed definitions do not require that the two signals contain different timing information, while Infineon's proposed definitions require that the second signal contain different information from the first.

1.   The Claim Language

Every asserted claim in the '214 patent (the double data rate invention) and the '804 patent (the delayed lock loop invention) contains the terms "first external clock signal" and "second external clock signal."[3] Most of the claims simply indicate that data is to be output on the bus in response to the first and second external clock signals. Three claims, however, reveal that the two clock signals can be used by the memory device to create an internal clock:

> 25.   The method of claim 15 further including generating at least one internal clock signal using the first and second external clock signals wherein the first amount of data corresponding to the first block size information is output onto the bus synchronously with respect to at least one internal clock signal.

'214 patent, claim 25.

> 26.   The method of claim 25 further including generating a first internal clock signal using a delay locked loop and the first and second external clock signals.

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[3]   See claims 1, 2, 4, 9, 10, 11, 15, 16, 18, 24, 25, and 26 of the '214 patent and claim 26 of the '804 patent.

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'214 patent, claim 26.

> 26. An integrated circuit device having at
> least one memory section which includes a
> plurality of memory cells, wherein the
> integrated circuit device outputs data on an
> external bus synchronously with respect to
> first and second external clock signals, the
> integrated circuit device comprises:
>
> . . . .
>
> Delay locked loop circuitry to generate an
> internal clock signal using the first and
> second external clock signals . . . .

'804 patent, claim 26.

The claim language thus indicates that somehow the memory

device is to use the information derived from the first and second

clock signal to create in internal signal. One must consult the

specification to understand how this is accomplished.

2. The Specification

In the "Background of the Invention" section, the

specification relates that one "object of this invention is to

provide a clocking scheme to permit high speed clock signals to be

sent along the bus with minimal clock skew between devices." '918

patent, col. 3, 11. 27-29. "The two clocks together provide a

synchronized high speed clock for all the devices on the bus."

'918 patent, col. 8, 11. 29-30. Most significantly, in the

"Clocking" subsection of the "Detailed Description," the inventors

explain:

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> Clocking a high speed bus accurately without
> introducing error due to propagation delays
> can be implemented by having each device
> monitor two bus clock signals and the[n]
> derive internally a device clock, the true
> system clock. The bus clock information can
> be sent on one or two lines to provide a
> mechanism for each bused device to generate an
> internal device clock with zero skew relative
> to all the other device clocks.

'918 patent, col. 18, l. 63 through col. 19, l. 4. This idea of

clock skew can be best understood by reference to Figures 8a and 8b

of the specification.

FIG_8A

FIG_8B

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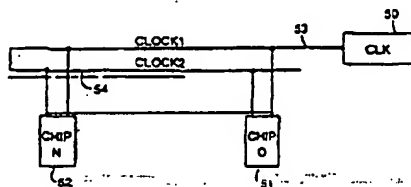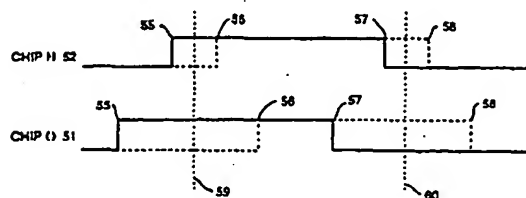
The specification clearly demonstrates how these figures represent
the two clock signals:

> Referring to FIG. 8a, in the preferred
> implementation, a bus clock generator 50 at
> one end of the bus propagates an early bus
> clock signal in one direction along the bus,
> for example on line 53 from right to left, to
> the far end of the bus. The same clock signal
> then is passed through the direct connection
> shown to a second line 54, and returns as a
> late bus clock signal along the bus from the
> far end to the origin, propagating from left
> to right. A single bus clock line can be used
> if it is left unterminated at the far end of
> the bus, allowing the early bus clock signal
> to reflect back along the same line as a late
> bus clock signal.

> FIG. 8b illustrates how each device 51,
> 52 receives each of the two bus clock signals
> at a different time (because of propagation
> delay along the wires), with constant midpoint
> in time between the two bus clocks along the
> bus. At each device 51, 52, the rising edge
> 55 of Clock1 53 is followed by the rising edge
> of 56 of Clock2 54. Similarly, the falling
> edge 57 of Clock1 53 is followed by the
> falling edge 50 of Clock2 54. This waveform
> relationship is observed at all other devices
> along the bus. Devices which are closer to
> the clock generator have a greater separation
> between Clock1 and Clock2 relative to devices
> farther from the generator because of the
> longer time required for each clock pulse to
> travers the bus and return along line 54, but
> the midpoint in time 59, 60 between
> corresponding rising of falling edges is fixed
> because, for any given device, the length of
> each clock line between the far end of the bus
> and that device is equal. Each device must
> sample the two bus clocks and generate its own
> internal device clock at the midpoint of the
> two.

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'918 patent, col. 19, 11. 4-32. See also Fig. 13 of the '918 patent (showing how the rising and falling edges of the two bus clocks can be synchronized).

In essence, this portion of the specification explains how chips N and O, which are located in different positions along the bus lines, receive the clock signals at different points in time due to their locations relative to the origin of the clock signal. By reflecting the signal along a second line, the memory system can compensate for this delay and create a second clock signal. From these two signals, chips N and O create an internal clock signal which corrects the clock skew caused by propagation delay. In order to correct the skew, the two signals must necessarily contain different information, as Rambus' expert admitted. See Markman Hearing, Tr. pg. pp. 296-298 (testimony of Dr. Huber). Although the specification lists this clocking scheme as a preferred embodiment, it is actually the only embodiment of the clock in the entire specification. As with the analysis of the term "bus," it is significant that the specification limits the clock to a single embodiment. See generally Wang, 197 F.3d at 1380; Toro, 199 F.3d at 1301; O.I. Corp., 115 F.3d at 1581.

3. The Extrinsic Evidence

The constructions taught by the specification are confirmed by the testimony of Mr. McAlexander who explained that to one ordinarily skilled in the art that the Rambus clock scheme allows

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the memory devices to sample each clock signal as it is received over the line and then averages the two signals such that every device is operating off the same clock, regardless of that device's location relative to the origin of the clock signal. Markman Hearing, Tr. pg. 457, line 2 to pg. 458, line 1 (testimony of Mr. McAlexander). Thus "the timing information and the difference between them is essential to this inventive concept of the clock design." Id."

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[38] Mr. McAlexander's testimony also explains how the clocking scheme comes full circle to the primary objective of the invention and the use of a multiplexed bus:

> In the prior art where the address information goes down one bus and data is responded to the bus on a totally different bus - so you have a data bus that's separate and distinct from the address bus - you could send down the control [or] the address information to a chip, activate it, . . . it goes in, finds the data from the storage cells and immediately sends it out to the data bus which is a separate bus.
>
> In the multiplexed design, the data must share the same bus as the address information. And so the . . . controlling system must assure that at no time does address or control information reside on the bus at the same time that data . . . is coming back on the bus; otherwise, you would end up with a collision.
>
> . . .
>
> So in order to arbitrate that and to make sure that nothing is on the bus when it's not supposed to be, the whole system has to be in sync. Every system, every . . chip, every component on the bus has to be operating under the exact same timing constraints.
>
> That's why it's important and valuable . . . to use a clock design that will synchronize everything together.

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In the interpretation of these terms, Rambus once again eschews the language of the specification, choosing to rely instead on the testimony of its expert who says that one skilled in the art would recognize that the first and second external clock signal can have, but does not need to have, different timing information in each signal. Therefore, according to Rambus, it is unnecessary to tie the claim definition to the language of the specification.[38] This approach runs afoul of the principle that the patent specification must always be reviewed to see if the patentee used the terms in a manner other than their ordinary meaning. Vitronics, 90 F.3d at 1582. Thus, even if one accepted Rambus' contention that the ordinary and accustomed meaning of first and external clock signals would be known to one of skill in the trade, the patent specification only describes a clocking scheme which corrects clock skew by creating an internal clock based on differing external clock signals.

4. Construction

Based on the claim language and the specification the term "first internal clock signal" is construed to mean "a periodic signal received by the memory device from an external source to

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Markman Hearing, Tr. pg. 465 l. 6 to pg. 466, l. 10.

[39] See Testimony of Dr. Huber, pg. 302, l. 25 - pg. 303 l. 2 ("I don't need to go to the patent to interpret the term. Clock signal is a well known term").

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provide first timing information." The term "second internal signal" is construed to mean "a periodic signal received by the memory device from an external source to provide second timing information that is different from the first timing information."

E.   Integrated Circuit Device

Lastly, the parties contest the meaning of "integrated circuit device" as that term is found in claim 26 of the '804 patent. Rambus contends that the term means a "circuit constructed on a single monolithic substrate, commonly called a 'chip.'" Infineon, however, argues that representations made in the prosecution of the '804 patent limit this term to "a device composed of integrated circuits that include at least an ID register and related interface and comparison circuitry."[40]

1.   The Claim Language And The Specification

Neither the claim language nor the specification inform the present inquiry. Indeed, the specification mentions an integrated circuit only once.

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[40] The parties have agreed that "integrated circuit device" is only disputed as it occurs in claim 26 of the '804 patent and not as it appears in the other patents. This is because the relevant file history limits the representations made to the PTO to only the '804 patent.

2. The File History

The file history of this claim is the only relevant category of intrinsic evidence. During the prosecution of Claim 26 in the '804 patent, (which was at that time, U.S. Patent App. 08/798,525 or the '525 application) Rambus expressly limited its claims by adding certain restrictions in order to overcome the PTO's prior art rejections. In response to the rejections, Rambus submitted new claims -- including the claim that ultimately issued as claim 26 of the '804 patent. Rambus argued to the PTO that the newly submitted claims were different from prior art because they all contained a device ID register and relevant interface and comparison circuitry limitations:

> The new claims submitted in this Supplemental Preliminary Amendment have been added to more definitely and fully protect Applicants' invention. <u>These newly submitted claims are directed to a memory device (or an integrated circuit having memory) having (1) an internal register for storing an identification value, (2) interface circuitry to receive a request on an external bus, and (3) comparison circuitry to determine whether the identification information in the request corresponds to the identification value in the internal register</u> - wherein when the identification information corresponds to the identification value, the memory device responds to the request.

Supplemental Preliminary Amendment, U.S. Patent App. 08/798,525, pp. 11-12. The '804 patent issued subsequently. Thus, it appears that Rambus believed that its claims did not cover devices without a device ID register and relevant interface and comparison

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circuitry. To allow Rambus to broaden its claim in the face of this restriction would defeat the public notice function of the patent history." In Hockerson-Halberstadt, Inc. v. Avia Group Intn'l, Inc., 222 F.3d 951 (Fed. Cir. 2000), the Federal Circuit explained:

> [The inventor's] argument therefore reduces to a request for a mulligan that would erase from the prosecution history the inventor's disavowal of a particular aspect of a claim term's meaning. Such an argument is inimical to the public notice function provided by the prosecution history. The prosecution history constitutes a public record of the patentee's representations concerning the scope and meaning of the claims, and competitors are entitled to rely on those representations when ascertaining the degree of lawful conduct, such as designing around the claimed invention. . . . Were we to accept [the inventor's] position, we would undercut the public's reliance on a statement that was in the public record and upon which reasonable competitors formed their business strategies.

Id. at 957 (internal citations omitted).

"Absent qualifying language in the remarks, arguments made to obtain the allowance of one claim are relevant to interpreting other claims in the same patent." Digital Biometrics, 149 F.3d at 1347. Rambus claims to have presented such "qualifying language" in a footnote of the above-quoted representation to the PTO, which mentions two of the inventive technologies claimed in this suit:

> The memory devices or integrated circuits having memory of the present invention may include additional and/or other inventive aspects, including, for example, delay lock loop circuitry and/or an internal register to

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> store a value which is representative of a
> number of clock cycles to transpire before the
> memory device responds to a read request.
> This "latency" register may be employed to
> control the timing of the output data after
> receipt of, for example, a read request.
> However it is noted that, in light of the July
> 27, 1998 Office Action and the rejection based
> on Weymouth, these additional and/or other
> inventive aspects, although forming a basis of
> patentability in their own right, will not be
> the focus of these Remarks.

Supplemental Preliminary Amendment, Patent App. No. 08/798,525, p.

12, n. 1. Rambus maintains that the express exclusion of the delay

locked loop system and the latency invention from the scope of the

attorney's remarks makes it "preposterous" to read a device ID

register limitation into the claims currently before the court.

Instead, during the Markman hearing in this case, Rambus' expert

Dr. Huber contended that the limitation applies to every other

claim of the patent (claims 1-25) but not claim 26. This

conclusion, according to Dr. Huber, is an obvious conclusion based

on the fact that claim 26 includes the inventive technologies

mentioned as additional and/or inventive features in the footnote.

Notwithstanding Rambus' current attempt to carefully craft its

limitations without much support in the patent history, the

footnote does not imply that the statement excludes claim 26, but

rather establishes that, in addition to the device ID register,

Rambus believed that it claims possessed other inventive features.

The last sentence of the footnote shows that Rambus chose not to

rely on those additional inventive features when distinguishing the

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claims from prior art. See id. ("these additional and/or other inventive aspects, although forming a basis for patentability in their own rights, will not be the focus of these Remarks"). Therefore, it is appropriate to read "integrated circuit device" as containing a device ID register, interface circuitry to receive a request from an external bus, and comparison circuitry to determine whether the identification information in the request corresponds to the identification register of the device.

Moreover, Rambus' suggested requirement that the integrated device be constructed on a single monolithic substrate is not supported by the specification and actually is undermined by the doctrine of claim differentiation. Claim 182 of the Preliminary Amendment to Patent App. No. 08/222,646, claim 6 of Patent No. 5,638,334 and claim 18 of Patent No. 5,657,481 all included the limitation that the device was "on a single semiconductor substrate." Claim 26 of the 804 patent contains no such limiting language and the doctrine of claim limitation warns against reading such a limitation into the disputed claim language unless the intrinsic evidence counsels otherwise.

3. Construction

Thus, the patent history supports the construction that an integrated circuit device, as used on claim 26 of the '804 patent, must have a device ID register, interface circuitry and comparison circuitry.

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III. The Extrinsic Evidence Generally: The Experts

The claim construction here has been accomplished largely without resort to extrinsic expert evidence, notwithstanding that the parties presented expert testimony addressing each disputed term. Having reviewed that testimony, the Court found it useful mostly in understanding the meaning of technical terminology other than the disputed terms as that terminology is used in the claims and specification. See Pitney Bowes, 182 F.3d at 1309 ("it is entirely appropriate, perhaps even preferable, for a court to consult trustworthy extrinsic evidence to ensure that claim construction it is tending to from the patent file is not inconsistent with clearly expressed, plainly apposite, and widely held understanding in the pertinent technical field").

As outlined in the substantive discussion of each term construed, Rambus pressed constructions that generally found little, if any, support in the claim language or the specification, depending in significant part upon the expert testimony of Dr. Huber whose testimony was generally at odds with the statements made by the inventors in the claims and specification. Thus, his extrinsic evidence had to be substantially disregarded as contradictory of the intrinsic evidence. Also, it was difficult to credit Dr. Huber's testimony on disputed terms because it reflected the general, and disturbing, tendency of Rambus to distance its current constructions from what the inventors said in making the

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claims and explaining the inventions in the specification,[41] and, in so doing, to use the claim construction process to broaden claims, rather clearly not made in the intrinsic evidence.

The record here, and the approach to claim construction taken by Rambus, illustrate the wisdom and importance of the rules of law that establish a hierarchal distinction between intrinsic and extrinsic evidence. On the other hand, the testimony of Mr. Joseph McAlexander, the expert offered by Infineon, was quite helpful and very credible because it was tethered closely to the intrinsic evidence and was not contradictory of the claim language or the specification. Notwithstanding that his testimony was reliable and informative it was ultimately not essential except as specifically cited in the construction. See Pitney Bowes, 182 F.3d at 1309 ("Although the patent file may often be sufficient to permit the judge to interpret the technical aspects of the patent properly, consultation of extrinsic evidence is particularly appropriate to ensure that his or her understanding of the technical aspects of the patent is not entirely at variance with the understanding of one skilled in the art").

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[41] Moreover, Dr. Huber left the impression that he was more an advocate than he was one generally knowledgeable in the field of the invention, notwithstanding his rather impressive curriculum vitae.

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CONCLUSION

For the foregoing reasons, the disputed terms in the four patents in suit are to be construed as reflected herein.

The Clerk is directed to send a copy of this Memorandum Opinion to all Counsel of Record.

It is so ORDERED.

Robert E. Payne
United States District Judge

Richmond, VA
Date: March 15, 2001

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
(Case No. P043D2C3C)

In the Application of:

FARMWALD et al.

Serial No: 09/492,982

Filed: JANUARY 27, 2000

Title: METHOD OF OPERATING A MEMORY
DEVICE HAVING A VARIABLE DATA
INPUT LENGTH

)
) Group
) Art Unit: 2818
)
) Before
) Examiner: T. Nguyen
)
)
)

Assistant Commissioner for Patents
Washington, DC 20231

AMENDMENT

Dear Sir:

Kindly amend the application as follows:

IN THE CLAIMS:

Please **substitute** the following claims for the pending claims

having the same claim number:

(A marked-up version showing insertions and deletions to the

pending claims is attached as EXHIBIT A)

1   1̶5̶1̶. (Amended) A method of controlling a memory device by a
2 memory controller, wherein the memory device includes a plurality of
3 memory cells, the method of controlling the memory device
4 comprises:
5   -- providing first-block size information to the memory device,
6 wherein the first block size information is provided by the memory
7 controller and is representative of a first amount of data to be input
8 by the memory device; and
9   issuing a first operation code to the memory device, wherein in
10 response to the first operation code, the memory device inputs the
11 first amount of data.

1   1̶5̶2̶. The method of claim 1̶5̶1̶ wherein the memory device inputs the
2 first amount of data synchronously with respect to an external clock
3. signal.

1   1̶5̶3̶. (Amended) The method of claim 1̶5̶1̶ further including:
2   providing second block size information to the memory device,
3 wherein the second block size information defines a second amount of
4 data to be input by the memory device; and
5   issuing a second operation code to the memory device, wherein in
6 response to the second operation code, the memory device inputs the
7 second amount of data.

1   1̶5̶4̶. (Amended) The method of claim 1̶5̶1̶ wherein the first block
2 size information and the first operation code are included in a request
3 packet.

1   1̶5̶5̶. (Amended) The method of claim 1̶5̶4̶ wherein the first block
2 size information and the first operation code are included in the same
3 request packet.

1   ~~156.~~ **6.** (Amended) The method of claim ~~151~~ **1** further including providing
2   the first amount of data to the memory device.

1   ~~157.~~ **7.** (Amended) The method of claim ~~156~~ **6** wherein the first amount
2   of data is provided to the memory device after a delay time transpires.

1   ~~158.~~ **8.** (Amended) The method of claim ~~157~~ **7** wherein the delay time is
2   representative of a number of clock cycles of an external clock signal.

1   ~~159.~~ **9.** (Amended) The method of claim ~~151~~ **1** wherein the first block
2   size information is a binary representation of the first amount of
3   data.

1   ~~160.~~ **10.** (Amended) The method of claim ~~151~~ **1** wherein the first amount
2   of data is output, by the memory controller, synchronously with respect
3   to an external clock signal and during a plurality of clock cycles of
4   the external clock signal.

1   ~~161.~~ **14.** (Amended) A method of operation in a synchronous memory
2   device, wherein the memory device includes a plurality of memory cells,
3   the method of operation of the memory device comprises:
4   receiving first block size information from a memory controller,
5   wherein the first block size information represents a first amount of
6   data to be input by the memory device in response to an operation code;
7   receiving the operation code, from the memory controller,
8   synchronously with respect to an external clock signal; and
9   inputting the first amount of data in response to the operation
10   code.

1   ~~162.~~ **15.** (Amended) The method of claim ~~161~~ **14** wherein inputting the first
2   amount of data includes receiving the first amount of data
3   synchronously with respect to the external clock signal.

16   X8
1   163. (Amended) The method of claim 162 wherein the first amount
2   of data is sampled over a plurality of clock cycles of the external
3   clock signal.

1   164. (Amended) The method of claim 161 wherein the first block
2   size information and the operation code are included in a request
3   packet.

1   165. (Amended) The method of claim 164 wherein the first block
2   size information and the operation code are included in the same
3   request packet.

1   166. (Amended) The method of claim 161 wherein the first block
2   size information is a binary representation of the first amount of data
3   to be input in response to the operation code.

1   167. (Amended) The method of claim 161 wherein the first amount
2   of data is output, by the memory controller, synchronously during a
3   plurality of clock cycles of the external clock signal.

1   168. (Amended) The method of claim 161 further including
2   generating an internal clock signal, using a delay locked loop and the
3   external clock signal wherein the first amount of data is input
4   synchronously with respect to the internal clock signal.

1   169. (Amended) The method of claim 161 further including
2   generating first and second internal clock signals using clock
3   generation circuitry and the external clock signal, wherein the first
4   amount of data is input synchronously with respect to the first and
5   second internal clock signals.

Page 4

1   23 [128]. The method of claim 22 [169] wherein the first and second internal

2 clock signals are generated by a delay lock loop.

1   29 [171]. (Amended) A method of operation of an integrated circuit,

2 wherein the integrated circuit includes a dynamic random access memory

3 array having a plurality of memory cells, the method of operation

4 comprises:

5   receiving block size information from a controller, wherein the

6 block size information represents an amount of data to be input in

7 response to an operation code;

8   receiving the operation code from the controller; and

9   inputting the amount of data in response to the operation

10 code.

1   30 [172]. (Amended) The method of claim 29 [171] further including storing

2 the amount of data in the memory array.

1   31 [173]. (Amended) The method of claim 29 [171] wherein the block size

2 information and the operation code are included in a request

3 packet.

1   32 [174]. (Amended) The method of claim 29 [171] wherein the block size

2 information is a binary representation of the amount of data to be

3 input in response to the operation code.

1   33 [176]. (Amended) The method of claim 29 [171] wherein the amount of data

2 is input, in response to the operation code, after a delay time

3 transpires.

1   34 [177]. The method of claim 33 [176] wherein the delay time is

2 representative of a number of clock cycles of the external clock

3 signal.

Kindly ADD the following claims:

11
178. (New) The method of claim 181 wherein the first operation
code is issued onto a bus.

12
179. (New) The method of claim 178 wherein the bus includes a
plurality of signal lines to multiplex control information, address
information and data.

13
180. (New) The method of claim 181 further including providing
address information to the memory device.

24
181. (New) The method of claim 161 wherein the operation code, the
first block size information and address information are included in a
packet.

25
182. (New) The method of claim 161 further including receiving
address information from the memory controller.

26
183. (New) The method of claim 161 wherein the first block size
information, and the operation code are received from an external bus.

27
184. (New) The method of claim 183 wherein the first block size
information, and the operation code are received from the same external
bus.

28
185. (New) The method of claim 184 wherein the external bus is
used to multiplex address information, control information and
data.

35
186. (New) The method of claim 184 further including receiving
address information from the controller.

Page 6

REMARKS

This Preliminary Amendment seeks to place this application in condition for allowance. New claims 178-186 have been added to more fully claim Applicant's invention. Several of the pending claims have been amended. No new matter has been added. In this regard, support may be found, for example, at page 22, line 11, to page 24, line 2, and page 27, lines 1-24 of the specification.

INFORMATION DISCLOSURE STATEMENT

In compliance with the duty of disclosure set forth in 37 C.F.R. §1.56, Applicants' submit concurrently herewith an Information Disclosure Statement (IDS) including modified Form PTO-1449. A copy of that IDS and modified Form PTO-1449 are attached hereto.

Some of the documents listed in the PTO-1449 have been cited by a defendant in an action pending in U.S. District Court For Eastern District of Virginia case, namely in _Rambus, Inc. v. Infineon Technologies A.G., et al._, as prior art against the inventions claimed in, among other patents, U.S. 6,034,918. The '918 patent is a parent of the instant application. Reference to these documents are listed on page 2 of the Defendents' AMENDED PRIOR ART NOTICE PURSUANT TO 35 U.S.C. §282 (hereinafter 'PRIOR ART NOTICE'). A copy of the PRIOR ART NOTICE is included with the IDS submission.

Furthermore, the construction or interpretation of a number of terms have recently been considered in a _Markman_ opinion issued in the above-mentioned litigation. A number of claims pending in the instant application incorporate or incorporated some of these terms including, for example, the terms "block size", "write request", and "bus". The term "write request" has been deleted from the pending claims (as amended). The term "bus" has been deleted from some of the pending claims (as amended). A discussion of "block size" may be found on pages 41-47 of the _Markman_ opinion, and a discussion of "bus" may be

Page 7

found on pages 17-41 of the *Markman* opinion. By submission of this *Markman* opinion, Applicants make no statement as to the correctness of the constructions set forth therein. Indeed, as is apparent from that opinion, the court substantially adopted the constructions proposed by Infineon, and not that construction proposed by Rambus. A copy of the *Markman* opinion is also included with the IDS submission.

CONCLUSION

Applicants request entry of the foregoing amendment. Applicants submit that all of the claims present patentable subject matter which definitely set forth the novel and unobvious features of Applicants' invention. Accordingly, Applicants respectfully request allowance of all of the claims.

It is noted that should a telephone interview expedite the prosecution in any way, the Examiner is invited to contact Neil Steinberg at 650-947-5325.

Respectfully submitted,

Date: April 26, 2001

Neil A. Steinberg
Reg. No. 34,735
650-947-5325

Page 8

1   151. (Amended) A method of controlling a memory device by a memory

2   controller, wherein the memory device includes a plurality of memory

3   cells, the method of controlling the memory device comprises:

4   providing first block size information to the memory device,

5   wherein the first block size information is provided by the memory

6   controller and [defines] is representative of a first amount of data to

7   be input by the memory device [in response to a write request]; and

8   issuing a first operation code [write request] to the memory

9   device, wherein in response to the first operation code, [write

10   request] the memory device inputs the first amount of data

11   [corresponding to the first block size information].

1   152. The method of claim 151 wherein the memory device inputs the

2   first amount of data synchronously with respect to an external clock

3   signal.

1   153. (Amended) The method of claim 151 further including:

2   providing second block size information to the memory device,

3   wherein the second block size information defines a second amount of

4   data to be input by the memory device [in response to a write request];

5   and

6   issuing a second operation code [write request] to the memory

7   device, wherein in response to the second operation code [write

8   request], the memory device inputs the second amount of data

9   [corresponding to the second block size information].

1   154. (Amended) The method of claim 151 wherein the first block

2   size information and the first operation code [write request] are

3   included in a request packet.

Page 9

1   155. (Amended) The method of claim 154 wherein the first block

2   size information and the first operation code [write request] are

3   included in the same request packet.

1   156. (Amended) The method of claim 151 further including providing

2   the first amount of data [corresponding to the first block size

3   information] to the memory device.

1   157. The method of claim 156 wherein the first amount of data is

2   provided to the memory device after a delay time transpires.

1   158. (Amended) The method of claim 157 [156] wherein the delay

2   time is representative of a number of clock cycles of [a] an external

3   clock signal.

1   159. (Amended) The method of claim 151 wherein the first block

2   size information is a binary representation of the first amount of data

3   [to be input in response to the first write request].

1   160. (Amended) The method of claim 151 wherein the first amount

2   of data [corresponding to the first block size information] is output,

3   by the memory controller, [input] synchronously during a plurality of

4   clock cycles of an [the] external clock signal.

1   161. (Amended) A method of operation in a synchronous memory

2   device, wherein the memory device includes a plurality of memory cells,

3   the method of operation of the memory device comprises:

4   receiving first block size information from a memory controller,

5   wherein the first block size information [defines] represents a first

6   amount of data to be input by the memory device in response to the

7   operation code [a write request];

Page 10

8   receiving <u>an operation code.</u> [a first write request] from the
9   <u>memory</u> controller<u>,</u> synchronously with respect to an external clock
10   signal; and
11   inputting the first amount of data [corresponding to the first
12   block size information] in response to the <u>operation code</u> [first write
13   request].

1   162. (Amended) The method of claim 161 wherein <u>inputting the first</u>
2   <u>amount of data includes receiving the first amount of data</u> [the first
3   amount of data corresponding to the first block size information is
4   sampled] synchronously with respect to the external clock signal.

1   163. (Amended) The method of claim 161 <u>wherein the first amount</u>
2   <u>of data is sampled synchronously during a plurality of clock cycles of</u>
3   <u>the external clock signal</u> [further including:
4   [receiving second block size information, wherein the second block
5   size information defines a second amount of data to be input in
6   response to a write request;
7   receiving a second write request from the bus controller; and
8   inputting the second amount of data corresponding to the second
9   block size information], in response to the second operation code write
10   request].

1   164. (Amended) The method of claim 161 wherein the <u>first</u> block
2   size information and the <u>operation code</u> [first write request] are
3   included in a request packet.

1   165. (Amended) The method of claim 164 wherein the <u>first</u> block
2   size information and the <u>operation code</u> [first write request] are
3   included in the same request packet.

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1   166. (Amended) The method of claim 161 wherein the first block
2   size information is a binary representation of the first amount of data
3   to be input in response to the <u>operation code</u> [first write
4   request].

1   167. (Amended) The method of claim 161 wherein the first amount
2   of data [corresponding to the first block size information] is [input]
3   <u>output, by the memory controller,</u> synchronously during a plurality of
4   clock cycles of [an] <u>the</u> external clock signal.

1   168. (Amended) The method of claim 161 further including
2   generating an internal clock signal using a delay locked loop and <u>the</u>
3   [an] external clock signal, wherein the first amount of data
4   [corresponding to the first block size information] is input
5   synchronously with respect to the internal clock signal.

1   169. (Amended) The method of claim 161 further including
2   generating first and second internal clock signals using clock
3   generation circuitry and [an] <u>the</u> external clock signal, wherein the
4   first amount of data [corresponding to the first block size
5   information] is input synchronously with respect to the first and
6   second internal clock signals.

1   170. The method of claim 169 wherein the first and second internal
2   clock signals are generated by a delay lock loop.

1   171. (Amended) A method of operation of an integrated circuit,
2   wherein the integrated circuit includes a ~~dynamic random access~~ memory
3   array having a plurality of memory cells, the method of operation
4   comprises:
5   receiving block size information from a controller, wherein the
6   block size information [defines a first] ~~represents an~~ amount of data

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7   to be input [from a bus] in response to <u>an operation code</u> [a write

8   request];

9   receiving <u>the operation code from the controller</u> [a first write

10   request]; and

11   inputting the [first] amount of data [corresponding to the block

12   size information] in response to the <u>operation code</u> [first write

13   request].

1   172. (Amended) The method of claim 171 further including storing

2   the [first] amount of data [corresponding to the block size

3   information] in the memory array.

1   173. (Amended) The method of claim 171 wherein the block size

2   information and the <u>operation code</u> [first write request] are included

3   in a request packet.

1   174. (Amended) The method of claim 171 wherein the block size

2   information is a binary representation of the [first] amount of data to

3   be input in response to the <u>operation code</u> [first write request].

1   176. (Amended) The method of claim 171 [161] wherein the [first]

2   amount of data is input, in response to [receipt of] the <u>operation code</u>

3   [first write request], after a delay time transpires.

1   177. The method of claim 176 wherein the delay time is

2   representative of a number of clock cycles of the external clock signal

3   [that transpire before the first amount of data is input].

1   178. (New) The method of claim 151 wherein the first operation

2   code is issued onto a bus.

Page 13

1   179. (New) The method of claim 178 wherein the bus includes a
2 plurality of signal lines to multiplex control information, address
3 information and data.

1   180. (New) The method of claim 151 further including providing
2 address information to the memory device.

1   181. (New) The method of claim 161 wherein the operation code, the
2 first block size information and address information are included in a
3 packet.

1   182. (New) The method of claim 161 further including receiving
2 address information from the memory controller.

1   183. (New) The method of claim 161 wherein the first block size
2 information, and the operation code are received from an external bus.

1   184. (New) The method of claim 183 wherein the first block size
2 information, and the operation code are received from the same external
3 bus.

1   185. (New) The method of claim 184 wherein the external bus is
2 used to multiplex address information, control information and
3 data.

1   186. (New) The method of claim 171 further including receiving
2 address information from the controller.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
(P043D2C3C)

In re Application of:)
)   RECEIVED
FARMWALD ET AL   )
)   Art Unit: MAY -2 2001
Serial No. 09/492,982   )   2818
)   TC 2800 MAIL ROOM
JANUARY 27, 2000   )
)   Examiner: T. Nguyen
Title: METHOD OF OPERATING A MEMORY DEVICE   )
         HAVING A VARIABLE DATA INPUT LENGTH   )

Commissioner of Patents and Trademarks
Washington, D.C. 20231

Dear Sir:

 With respect to the above-identified application, transmitted herewith is an AMENDMENT (14 pages) + attachment and an INFORMATION DISCLOSURE STATEMENT (2 pages), modified PTO form 1449 (2 pages) and copies of references cited in the modified PTO form 1449.

The fee has been calculated as shown below:

CLAIMS AS AMENDED						
	Claims Remaining After Amendment	Highest Number Previously Paid For	Extra	Rate		
				Large Entity	Small Entity	Amount
Number of Claims In Excess of 20	46	38	8	$ 18.00	$ 9.00	$144.00
Independent Claims In Excess of 3	3	3	0	$ 80.00	$ 40.00	$0.00
First Presentation of Multiple Dependent Claims				···250.00	··125.00	·0·
Submission of Information Disclosure Statement under 37 CFR §1.97(b)						-0-
					TOTAL FEE DUE:	$144.00

[XX] Please charge my Deposit Account No. 50-0998 in the amount of $ 144.00   to cover the above fees. A duplicate copy of this sheet is enclosed.

[XX] The Commissioner is hereby authorized to charge any fees which may be required, or credit any overpayment to Deposit Account No. 50-0998. A duplicate copy of this sheet is enclosed.

04/30/2001 TGEDAMUI 00000120 500998 09492982
01 FC:103   144.00 CH

Date: _April 26, 2001_

Respectfully submitted,

By: _____
Neil A. Steinberg
Registration No. 34,735
650-947-9325

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

(Case No. RA043D2C3C)

In the Application of:

FARMWALD et al.

Serial No: 09/492,982

Filed: JANUARY 27, 2000

Title: METHOD OF OPERATING A MEMORY
DEVICE HAVING A VARIABLE DATA
INPUT LENGTH

Group·
Art Unit: 2818

Before
Examiner: T. Nguyen

Assistant Commissioner for Patents
Washington, DC 20231

Certificate of Mailing Under 37 CFR 1.8

I hereby certify that the attached **1) Transmittal (1 copy in duplicate)**

2) Amendment (14 pages + 4 page attachment) and **3) Information Disclosure**

Statement (2 pages) + modified form PTO 1449 (2 pages) and copies of references

cited in the modified form PTO 1449 is/are being deposited with the United States

Postal Service with sufficient postage as first class U.S. mail in an envelope addressed

to:

Assistant Commissioner for Patents
Washington, D.C. 20231

On April 26 , 2001.

_____
(Signature)

Neil Steinberg
(Print Name of Person Signing Certificate)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
(Case No. P043D2C3C)

In the Application of:)
) Group
     FARMWALD et al.   ) Art Unit: 2818
)
Serial No: 09/492,982   ) Before
) Examiner: T. Nguyen
Filed: JANUARY 27, 2000   )
)
Title: METHOD OF OPERATING A MEMORY   )
       DEVICE HAVING A VARIABLE DATA   )
       INPUT LENGTH   )

FACSIMILE COVER SHEET

DATE: May 10, 2001

TO: Examiner: T. Nguyen

FAX NUMBER: (703)-308-7724

NO. OF PAGES: 22 including this cover sheet

OFFICIAL FILING

The attached:

     Information Disclosure Statement (in duplicate) + PTO-1449 + attachments
     (21 pages)

is/are being facsimile transmitted to the United States Patent and Trademark Office (703) 308-6296 on
May 10, 2001 in the above-referenced application.

                         Respectfully submitted,

                         Joe G. Moniz
                         Rambus Inc.
                         Phone: 650-947-5336
                         Fax: 650-947-5001

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
(Case No. P043D2C3C)

In the Application of:	)	Group
	)	Art Unit: 2818
FARMWALD et al.	)	
	)	Before
Serial No: 09/492,982	)	Examiner: T. Nguyen
	)	
Filed: JANUARY 27, 2000	)	
	)	
Title: METHOD OF OPERATING A MEMORY	)	
DEVICE HAVING A VARIABLE DATA	)	
INPUT LENGTH	)	

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(Name of Person Mailing Correspondence)

Signature _____ Date _____

Assistant Commissioner for Patents
Washington, DC 20231

INFORMATION DISCLOSURE STATEMENT

FAX COPY RECEIVED

MAY 1 0 2001

Dear Sir:

Applicants submit concurrently herewith an Information Disclosure Statement (IDS) citation Form PTO-1449, including a reference identified in the IDS submitted previously on Nov. 17, 2000, but not noted (by way of, for example, the Examiner's initials) by the Examiner as being formally considered.

It is respectfully requested that the Examiner make his consideration of this reference formally of record with the next Action. The Commissioner is hereby authorized to charge Applicants' Deposit Account No. 50-0998 for any fee required in connection with this submission. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

Date: May 10, 2001

Neil A. Steinberg
Reg. No. 34,735
650-947-5325

(Case No. P043D2C3C)

In the Application of:	) Group
	) Art Unit: 2818
FARMWALD et al.	)
	) Before
Serial No: 09/492,982	) Examiner: T. Nguyen
	)
Filed: JANUARY 27, 2000	)
	)
Title: METHOD OF OPERATING A MEMORY	)
DEVICE HAVING A VARIABLE DATA	)
INPUT LENGTH	)

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to the Commissioner of Patents and Trademarks, Washington, D.C. 20231 on _____

(Name of Person Mailing Correspondence)

_____   _____
Signature   Date

Assistant Commissioner for Patents
Washington, DC 20231

INFORMATION DISCLOSURE STATEMENT

RECEIVED

MAY 1 0 2001

Dear Sir:

Applicants submit concurrently herewith an Information Disclosure Statement (IDS) citation Form PTO-1449, including a reference identified in the IDS submitted previously on Nov. 17, 2000, but not noted (by way of, for example, the Examiner's initials) by the Examiner as being formally considered.

It is respectfully requested that the Examiner make his consideration of this reference formally of record with the next Action. The Commissioner is hereby authorized to charge Applicants' Deposit Account No. 50-0998 for any fee required in connection with this submission. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

Date: May 10, 2001

Neil A. Steinberg
Reg. No. 34,735
650-947-5325

Not found in USPTO file:

FORM PTO-1449

(54) Name of Invention: Method for Setting Memory Access Timing

(72) Inventor: Takashi Saito
Mitsubishi Electric Company, Ltd., Computer Manufacturing Facilities
325 Uemachiya, Kamakura City, Kanagawa Prefecture
(71) Applicant: Mitsubishi Electric Company, Ltd.
2-2-3 Marunouchi, Chiyoda-ku, Tokyo
(74) Representative: Masao Oiwa, Patent Attorney, and two others

Details

1. Name of Invention

    Method for Setting Memory Access Timing

2. Patent Claims

    A method for setting memory access timing in a logical circuit that accesses memory, characterized by the provision of a register for which a variety of values can be set by a program, by repetitively having the value set in said register be changed sequentially by the program and performing test writes to the memory and test reads from the memory where the data that is written is compared to the data that is read, by setting to the register the setting that was in effect when the results of the comparison matched, and by accessing the memory based on said setting.

1.   Detailed Explanation of the Invention

(Area of Application in Industry)

This invention pertains to a method for setting the memory access timing in order to set the access timing for random access memory (hereinafter abbreviated "RAM") that is equipped in, for example, data processing devices.

[Prior Art]

Figure 6 shows a block diagram of the logic circuits that use the conventional memory access timing set method. In the figure, 1 is RAM (using the example where a dynamic RAM is used), 2 is an address multiplexer, 3 is a multiplexed address bus connecting the RAM 1 with the address multiplexer 2, 4 is an address bus connected to the address multiplexer 2, 5 is a data bus connected to the RAM 1, and 6 is a memory control ring. In addition, 7 is a flipflop for generating the row address select signal (RAS signal), hereinafter abbreviated "RAS flipflop," 8 is a flipflop for generating the column address select signal (CAS signal), hereinafter abbreviated "CAS flipflop." 9 is a flipflop for generating the column select signal (COLS signal), hereinafter abbreviated "COLS flipflop." 10 is an AND gate. 11, 12, and 13 are OR gates, 14, 15, and 16 are NOR gates, and 17, 18, 19, and 20 are jumper lines for selecting the output from the memory control ring 6 that is to be used. Additionally, for simplicity in the explanation, the logic circuits for refreshing the RAM 1 are not shown.

The operation of this method is described below. In this explanation, "1" indicates either the active level or the high logic level, while "0" indicates the inactive level or the low logic level. The memory control ring 6 is enabled and placed in an operational state when the memory access mode signal of line L1 goes to "1," and, synchronized to the master clock on line L2, the outputs T0, T1.... Tk.... Tl...., Tm.....Tn..., Te-1, Te are sequentially set to "1" in the state transitions. When the memory access mode signal is "0," all outputs T0 to Te from the memory control ring 6 go to "0." The respective flipflops 7, 8, and 9 each output their latched signals from the output terminal 1 on each, and output the inverse of the latched signal on output terminal 0 of each. The RAS signal, CAS signal, and WE signal applied, respectively, to the RAS, CAS, and WE terminals of RAM 1 are each active at "1." In addition, in this conventional example, jumper lines 17, 18, 19, and 20 are set by hand, selecting, respectively, outputs Tk, Tl, Tm, and Tn of the memory control ring 6.

Below will be explained an example of an operation to write to the RAM 1, referencing the timing chart shown in Figure 4. When the memory access commences, both the memory access mode signal on Line L1 and the write mode signal on Line 3 both go to "1." At this time, the address is applied to the address bus 4, the row address is selected by the address multiplexer 2 and is output on the multiplexed address bus 3. At this time the write data is applied to data bus 5.

In this way, the row address and write data are applied, and, as described above, the memory access mode signal of line L1 is at "1," so the memory control ring 6 commences operations, and there are state transitions so that outputs T0, T1, ... Tk sequentially go to "1." When Tk goes to "1," the "1" output Tk is applied to terminal D of the RAS flipflop 7 through the jumper line 17 and OR gate 11, and when output Tk + 1 of memory control ring 6 goes to "1," the RAS signal that is output from output terminal 1 of the RAS flipflop 7 goes to "1." In addition, at this time the inverted signal that is output from the output terminal 0 of the RAS flipflop 7 goes to "0," causing the output of the NOR gate 14 to go to "1," and the output of the OR gate 11 to go to "1," causing the output of the RAS flipflop 7, or in other words the RAS signal, to be held at "1" even if the memory control ring 6 status advances. When the "1" output of the memory control ring 6 transitions from T1 to T1 + 1, the same operation as described above causes the COLS signal, which is the output of the COLS flipflop 9, to be held at "1." This COLS signal causes the address multiplexer 2 to output the column address to the multiplexed address bus 3, and the output of the AND gate 10, or in other words the WE signal that is applied to the RAM 1 terminal WE, goes to "1," placing RAM 1 in write mode. When the "1" output of the memory control ring 6 transitions from Tm to Tm + 1, a operation similar to what was described above causes the output of the CAS flipflop 8, or in other words the CAS signal, to be held at "1." As described above, the RAS signal, the CAS signal, the WE signal, and the COLS signal all go to "1," putting all conditions in place to write to the RAM 1; hence the data write operation is performed, the status of the memory control ring 6 advances, and the write operation is concluded at the point in time where the output Tn - 1 goes to "1." When the output Tn of the memory control ring 6, or in other words the memory access complete signal on line 4, goes to "1" followed by the output Tn + 1 going to "1," the memory access mode signal on line L1 and the write mode signal on line L3 both go to "0," causing the outputs of the NOR gates 14, 15, and 16, along with the outputs of the OR gates 11, 12, and 13 to go to "0"; consequently, the RAS signal, the CAS signal, and the COLS signal all go to "0," completing the operation for writing to the RAM 1. Note that TW shown in Figure 4 is the period over which the write mode conditions are fulfilled by the control signals to the RAM 1 (i.e., the memory access mode signal, the write mode signal, the RAS signal, the COLS signal, the CAS signal, and the WE signal).

On the other hand, in the operations to read from the RAM 1, as shown in Figure 5, the write mode signal and the WE signal go to "0," and at the point in time when the output Tn - 1 of the memory control ring 6 ceases to output "1," or in other words, at the point in time when the output Tn goes to "1," the output data that is read from the RAM 1 is assumed to be set, and with the output Tn, the data on the data bus 5 is accepted. At this time, when, in operations similar to the write operations described above the output Tn + 1 of the memory control ring 6 is to go to "1," all control signals become inactive and the operations to read from the

RAM 1 are terminated. Note that the TR shown in Figure 5 is the period of time over which the control signals to the RAM 1 fulfill the read mode conditions.

[Problems Solved by this Invention]

In the conventional method for setting the memory access timing, the part that sets the RAM access timing is set by jumper lines, and thus it requires a manual intervention to set the jumper lines. Additionally, generally RAMs have a variety of different access times, and when the type of RAM that is used is changed it is necessary to change the settings of the jumpers in order to change the access timing, and, as a result, the RAM cannot be accessed correctly if the setting is incorrect or there may also be the problem that, even if RAM that can operate at high speeds is used, the actual performance of the RAM will not be good if the access timing used is for low speed RAM.

This invention was created in order to solve the types of problems described above, and its objective is to provide a method of setting the memory access timing that automatically sets the access timing without any manual intervention, making it possible to exploit the full capabilities of the RAM and to improve reliability.

[Method by Which the Problems are Solved]

The method of setting the memory access timing in this invention is characterized by the logic circuits that access the memory (RAM 1) being equipped with registers 21, 22, 23, and 24 that can be set to a variety of values by a program, where the values that are set to these registers 21, 22, 23, and 24 are repetitively changed sequentially by the program at which time test data is written to and read from the memory (RAM 1) and comparisons are made between the write data and the read data where the values that were set when the results of the comparison indicates a match are set to registers 21, 22, 23, and 24, so that the access to the memory (RAM 1) is performed based on these settings.

[Operation]

The registers 21, 22, 23, and 24 in this invention are set to any given value by the program, and the memory (RAM 1) is accessed based on the various settings that have been set, at which time test data is written to the memory and read from the memory. The data written as this test data, and the data that is read, are compared to each other for each of the access operations that are based on the respective settings, and when the data that is written to the memory (RAM 1) matches the data that is read from the memory, then the settings are set as the final settings in the registers 21, 22, 23, and 24, and after that time the access timing is determined based on these final settings and the memory (RAM 1) is accessed with that access timing when the specific data write and data read operations are performed.

[Example of Embodiment]

An Example of Embodiment of this invention is explained below based on the figures. Figure 1 is a block diagram of logic circuits that use the method for setting the memory access timing in this Embodiment of the invention. In Figure 1 the same symbols are used as corresponding to the structural elements shown in Figure 5, so the explanations are omitted here. In Figure 1, 21 is the register for determining the timing with which the RAS signal is produced (hereinafter termed the "RAS register"), 22 is the register for determining the timing with which the COLS signal is produced (hereinafter termed the "COLS register"), 23 is the register for determining the timing with which the CAS signal is produced (hereinafter termed the "CAS register"), 24 is the register for determining the timing with which the memory access complete signal will be produced (hereinafter termed the "CPLT register"). 25, 26, 27, and 28 are the selectors that select one output from output T0 to Te of the e + 1 registers in memory control ring 6.

Next the operation will be explained. Let us assume that there are five different types of RAM that can be obtained, and, the access timing on these types of RAM, from fastest to slowest, are RAM_1, RAM_2, RAM_3 RAM_4, and RAM_5. The respective RAMs can be accessed correctly by outputting the RAS signals, COLS signals, CAS signals, and memory access complete signals shown in the timing diagram of Figure 2. The explanation described below considers the operations when RAM_3 is installed.

The table has the settings for the RAS register 21, the COLS register 22, the CAS register 23, and the CPLT register 24, or in other words, the settings for k1 to k5, l1 to l5, m1 to m5, and n1 to n5 in Figure 2, are stored as a table. This program executes the flow chart shown in Figure 3. In other words, the program is executed (Step S1), the pointer indicates RAM_1 (Step S2), the information indicated by the pointer (in this case, the settings k1 corresponding to RAM_1 shown in Figure 2) are loaded into RAS register 21 (Step S3), the pointer is then incremented (Step S4), the information indicated by the pointer (in this case, the setting l1 corresponding to RAM_1) is loaded into the COLS register 22 (Step S5), the pointer is incremented (Step S6), the information indicated by the pointer (in this case, the setting m1 corresponding to RAM_1) is loaded into the CAS register 23 (Step S7), the pointer is incremented (Step S8), the information indicated by the pointer (in this case the setting n1 corresponding to RAM_1) is loaded into the CPLT register 24 (Step S9), the pointer is incremented (Step S10), the test data is written into the RAM_3 (because in this case it is RAM_3 that is installed) (Step S11), and the write operation is performed with the timing shown in Figure 4. Then the data is read from the RAM_3 with the timing shown in Figure 5 (Step S12), and the data that was read is compared to the data that was written (Step S13). In this case, the settings are the settings k1, l1, m1, and n1 that correspond to RAM_1. These settings do not match the timing for the control signals (the RAS signal, the COLS signal, the CAS signal, and the memory access complete signal) for RAM_3, so the comparison in Step 13 of the data that was read and the data that

was written does not indicate a match with this timing. As a result, the program continues to Step S14, and a check is made for a pointer error. If there is an error then an error report is made (Step S15), and if there is no error, then the program returns to Step S3.

The information indicated by the pointer when the program returns to Step S3 is the setting k2 that corresponds to the RAM₂ that is installed, and this setting k2 is loaded into the RAS register 21. After that, the same process that is described above is performed (Steps S4 through S10) and the setting I2 is loaded into the COLS register 22, the setting m2 is loaded into the CAS register 23, the setting n2 is loaded into the CPLT register 24, the test data is written to the RAM₂ (Step S11) the data is read from the RAM₂ (Step S12), and the data that was written is compared to the data that was read (Step 13). In this case, the RAM access timing is set so that, when the operations for writing and reading the specified data are performed, the settings k2, I2, m2, and n2 correspond to RAM₂, and thus RAM₂ is accessed with the appropriate timing and the data that was read matches the data that was written so the program continues to Step 16 and the settings k2, g2, m2, and n2 are set into registers 21, 22, 23, and 24 as the final settings, and selectors 25, 26, 27, and 28 cause the RAS signal to be "1" when the output Tk2 + 1 of the memory control ring 6 is "1," the COLS signal to be "1" when the output Tl2 + 1 is "1," the CAS signal to be "1" when the output Tm2 + 1 is "1," and the memory access complete signal to be "1" when the output Tn2 is "1." In addition, when the output Tn2 + 1 is "1" the RAS signal, the COLS signal, the CAS signal and the memory access complete signal all go to "0."

While the explanation of the flow chart was based on the assumption that RAM 2 was installed, if RAM₁, RAM₃, RAM₄, or RAM₅ were installed instead, the processes in Steps 3 through 13 would be performed once, three times, four times, or five times, respectively, to set the access timing.

Because in the Example of Embodiment described above, it is possible to change the access timing using a program, it is easy to perform RAM access timing margin tests. In addition, although the timing will be that for the type of RAM with the slowest access time, even if a mixture of RAMs with different access times are installed in the logic circuits, the RAM can still be accessed correctly. In addition, if in high-speed computers, the RAM access timing is set individually by the card unit or the bank unit of main memory, then even if the type of RAM is different on different card units or bank units, the timing can be performed to match the capability of the RAM, making it possible to prevent any impediments to performance by mixing types of RAM. Additionally, in the program that determines the settings, it is possible to set the access timing that is optimized for the RAM that is installed and that is able to fully exploit the capabilities of the RAM through selecting the optimal values through changing the settings in even finer increments, rather than determining the settings in such a way as to compensate for the minor timing differences between the various RAM manufacturing locations. If in the program access timing setting checks are

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/492.982	01/27/00	FARMWALD	M P043D2C3C

MMC2/0522

EXAMINER
NGUYEN, T

ART UNIT	PAPER NUMBER
2818	

NEIL A STEINBERG ESQ
RAMBUS INC
4440 EL CAMINO REAL
LOS ALTOS CA 94022

DATE MAILED:
05/22/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

	Application No.	Applicant(s)
Office Action Summary	09/492,982	FARMWALD ET AL.
	Examiner	Art Unit
	Ten T. Nguyen	2818

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on <u>27 April 2001</u> .

2a) ☐ This action is FINAL.   2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) <u>151-174 and 176-186</u> is/are pending in the application.

   4a) Of the above claim(s) <u>1-150 and 175</u> is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) <u>151-174 and 176-186</u> is/are rejected.

7) ☒ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   a) ☐ All b) ☐ Some * c) ☐ None of:

   1. ☐ Certified copies of the priority documents have been received.

   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .

   3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

   * See the attached detailed Office action for a list of the certified copies not received

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☐ Notice of References Cited (PTO-892)

16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

17) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) <u>17-19,21</u> .

18) ☐ Interview Summary (PTO-413) Paper No(s). _____ .

19) ☐ Notice of Informal Patent Application (PTO-152)

20) ☐ Other: _____

U.S. Patent and Trademark Office
PTO-326 (Rev. 01-01)   Office Action Summary   Part of Paper No. 22

1.   The following action is in response to the amendment filed by Applicants on April

27, 2001.

2.   Claim 151-174 and 176-177 are pending.

        New claims 178-186 have been added.

3.   The Information Disclosure Statements submitted by Applicants on February 12,

2001, March 12, 2001, April 27, 2001 and May 10, 2001 have been received and fully

considered.

4.   Claims 151-174 and 176-186 are rejected under 35 U.S.C. 112. first paragraph,

as containing subject matter which was not described in the specification in such a way

as to enable one skilled in the art to which it pertains, or with which it is most nearly

connected, to make and/or use the invention. Applicants failed to provide an adequate

written description of how the memory controller provides the block size information to

the memory device.   The Examiner was unable to find the support for the memory

controller in the specification.

5.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless —
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public
> use or on sale in this country, more than one year prior to the date of application for patent in the United
> States.

6.   Claims 151-153, 156, 159-162, 166-167, 171-172, 174, 178. 180, 182-184, 186,

as best understood, are rejected under 35 U.S.C. 102(b) as being anticipated by Laid

Open Patent Application Sho 60-55459 (hereinafter JP '459).

        JP '459 disclosed in figures 4-5 a memory control device [2] for controlling the

block data transfer to and from memory [1]. In page 6, JP]459 disclosed a method for write access wherein a function signal [231] and data [233] from the access origin are set in a function register [209] and a write data register [207]. If block data transfer control circuit [206] decodes the contents of function register [209] and detects that it is a write request for the transfer origin address, the content of write data register [207] are set in transfer destination address counter [202], and response [230] is transferred to the access origin (page 6, lines 34-38). JP '459 further disclosed as the memory function signal [241] is made the write mode, and the contents of transfer destination address counter [203] are output as memory address signal [242]. memory data [243] is transferred to and stored at the transfer destination memory area (page 7, lines 32-34).

7.   Claims 154-155, 157-158, 163-165, 168-170, 173, 176-177, 179, 181, 185 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112. second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.
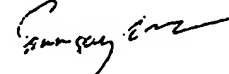
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tan T. Nguyen whose telephone number is (703) 308-1298. The examiner can normally be reached on Monday to Friday from 08:00 AM to 04:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Nelms, can be reached on (703) 308-4910. The fax phone number for the organization where this application or proceeding is assigned is (703) 308-7724.

Application/Control Number: 09/492,982　　　　　　　　　　　　　　Page 4
Art Unit: 2818

　　　Any inquiry of a general nature or relating to the status of this application or

proceeding should be directed to the receptionist whose telephone number is (703) 308-

0956.

Tan T. Nguyen
Primary Examiner
Art Unit 2818

#23 Response
(w/attack
(signature)
6/6/01

Ty

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
(Case No. P043D2C3C)

In the Application of:)
) Group
      FARMWALD et al.) Art Unit: 2818
)
Serial No: 09/492,982) Before
) Examiner: T. Nguyen
Filed: JANUARY 27, 2000)
)
Title: METHOD OF OPERATING A MEMORY)
      DEVICE HAVING A VARIABLE DATA)
      INPUT LENGTH)

Box: No Fee

FACSIMILE COVER SHEET

DATE: June 1, 2001

TO: Examiner: T. Nguyen

FAX NUMBER: (703)-308-7724

NO. OF PAGES: 15 including this cover sheet

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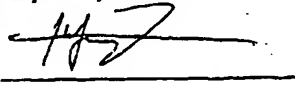
OFFICIAL FILING

The attached:

RESPONSE TO OFFICE ACTION
(14 pages)

is/are being facsimile transmitted to the United States Patent and Trademark Office (703) 308-7724 on June 1, 2001 in the above-referenced application.

Respectfully submitted,

Joe G. Moniz
Rambus Inc.
Phone: 650-947-5336
Fax: 650-947-5001

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
(Case No. P043D2C3C)

In the Application of:)
)
    FARMWALD et al.   )
)   Group
Serial No: 09/492,982   )   Art Unit: 2818
)
Filed: JANUARY 27, 2000   )   Before
)   Examiner: T. Nguyen
Title: METHOD OF OPERATING A MEMORY   )
       DEVICE HAVING A VARIABLE DATA   )
       INPUT LENGTH   )

Assistant Commissioner for Patents
Washington, DC 20231

BOX: NO FEE

RESPONSE TO OFFICE ACTION

Dear Sir:

In the Office Action mailed May 22, 2001, claims 151-174 and 176-
186 have been rejected under 35 U.S.C. §112, first paragraph as
containing subject matter not described in the specification in such a
way as to enable one skilled in the art to which it pertains, or with
which it is most nearly connected, to make and/or use the invention.
Furthermore, claims 151-153, 156, 159-162, 166-167, 171-172, 174, 178,
180, 182-184, and 186 have been rejected as being anticipated by
Japanese Laid-Open Patent Application No. 60-55459 (hereinafter "the
'459 Application"). Each rejection is addressed separately below.

Rejection - 35 U.S.C. § 112, first paragraph:

Claims 151-174 and 176-186 have been rejected under 35 U.S.C. §112, first paragraph, in that Applicants failed to provide an adequate written description of how the memory controller provides block size information to the memory device. Applicants respectfully disagree.

The specification of the above-referenced application describes a method of controlling a memory device by a memory controller. (See, for example, page 13, lines 13-17). In one embodiment, this method of controlling includes providing block size information to the memory device wherein the block size information is representative of an amount of data to be input by the memory device. (See, page 22, lines 7-10 ("The last byte contains ... BlockSize [0:3] ...."); page 27, lines 23-30 (the block size information "specifies the size of the data block transfer"); and page 20, line 23 to page 21, line 1, (the memory device "... accept[s] data from the master (in the case of a write request) in a data block transfer."); in addition, see page 74, lines 1-31).

One type of encoding scheme for the block size is described on page 27, line 24 to page 28, line 11 of the specification. In this regard, the application states:

> Blocksize[0:3] specifies the size of the data block transfer. If BlockSize[0] is 0, the remaining bits are the binary representation of the block size (0-7). If BlockSize[0] is 1, then the remaining bits give the block size as a binary power of 2, from 8 to 1024. A zero-length block can be interpreted as a special command, for example,

to refresh a DRAM without returning any data, or to change
the DRAM from page mode to normal access mode or vice-versa.
(page 27, lines 23-30).

The applications notes, however, that "[p]ersons skilled in the art
will recognize that other block size encoding schemes or values can be
used." (page 28, lines 13-14).

Thus, Applicants respectfully submit that the application, as
filed, provides an adequate written description of how a controller or
master controls a memory device, in connection with a write operation,
via providing block size information to the memory device.

Rejection - 35 U.S.C. §102(b):

The pending rejection under 102(b), in view of the '459
application, is substantively identical to the rejection set forth in
the Office Action dated August 1, 2000, wherein the Examiner rejected
the then pending claims, under 35 U.S.C. §102(b), based on the '459
Application. This rejection was addressed in the Amendment dated
October 31, 2000. The rejection was believed to be overcome, as
demonstrated by the Notice of Allowance mailed November 28, 2000.[1]

It is respectfully submitted that the '459 Application does not
anticipate claims 151-153, 156, 159-162, 166-167, 171-172, 174, 178,

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[1]By way of note, in a telephone interview on November 21, 2000,
the Examiner expressed a concern that claim 151 could be interpreted in
such a way as to read on the '459 Application. Applicants submitted an
Amendment on November 22, 2000 to address the Examiner's concern. A
Notice of Allowance was mailed on November 28, 2000.

Page 3

180, 182-184, and 186.[2] In this regard, memory 1 disclosed in the '459 Application -- unlike the claimed invention -- is not provided nor does it receive information indicating the "number of words to transfer"[3] as required by the claims of the instant application. For example, claim 161 recites in pertinent part:

> A method of operation in a synchronous memory device, ... the method of operation of the memory device comprises:
>   receiving first block size information from a memory controller, wherein the first block size information represents a first amount of data to be input by the memory device in response to an operation code;

The memory in the '459 Application does not receive block size information. Rather, memory 1 of the '459 Application responds to the sequentially applied address and control signals from the memory control device 2 in order to store the appropriate number of words.

It is the memory control device 2 of the '459 Application which receives, decodes and stores the information indicating the number of words to be stored in memory 1. The memory control device 2 stores the number of words in a counter, and, based thereon, generates and sequentially applies the appropriate address and control signals necessary to write the words to memory 1. The information indicating

---

[2]The discussion below is very similar to the discussion set forth in the October 31, 2000 Amendment.

[3]For the purposes of this discussion, the phrase "number of words to transfer" may be assumed to correspond to "block size information".

the number of words to transfer is not provided to memory 1 (and as such, memory 1 does not receive such information).

The '459 Application

The '459 Application discloses a system including memory 1, memory control device 2, cache memory 3, a main processing device 4, and an input/output processing device 5. (See Figure 2). The memory 1 is connected to memory control device 2 via memory bus 6. Memory control device 2 and input/output processing device 5 are both connected to bus 7 (See, the '459 Application, page 3 lines 11-16, and Figure 2).

Communication between memory 1 and devices connected to bus 7 is executed via memory control device 2. In this regard, the '459 Application states that "control of reading or writing from memory 1 is performed by memory control device 2 via memory bus 6" (page 3, line 13-14). The memory control device 2 controls memory 1 via a memory interface which includes memory address signal 242, memory data [bus] 243 and memory response signal 240. (See, the '459 Application, page 6, lines 17-21). Address signal 242 and data 243 are employed to transfer address and data, respectively, between memory control device 2 and memory 1. (See, the '459 Application, page 6 lines 18-21 and Figure 6).

In operation, a "number of words to transfer," together with origin and destination addresses, are provided to memory control device 2. (See, e.g., the '459 Application, page 4, lines 36-39). Memory control device 2 increments or decrements source and destination

Page 5

address counters while maintaining a count of the number of remaining words to be transferred to memory 1. In this regard, the '459 Application, on page 5, lines 21-24 states:

> The counter for the remaining number of words to transfer, which is set with number of words to transfer, is decremented each time data is transferred and stored, and when that count value reaches zero, transfer ... ends.

The memory control device 2 of the '459 Application, at all times, maintains the information regarding the number of words to transfer, generates the appropriate control and address signals, and applies the control and address signals which are necessary to transfer the requested number of words to memory 1. (See, the '459 Application, page 7, lines 26-39, and Figure 9). The memory control device 2 receives, decodes and stores, in a counter 203, information indicating the number of words to transfer to memory 1 and, based thereon generates address and control signals and sequentially applies those addresses and control signals in order to transfer the indicated number of words from memory 1. The memory control device 2 does not provide information indicating the number of words to transfer to memory 1.

Although the '459 Application does not describe memory 1 in great detail,[4] memory 1 is most likely a standard off-the-shelf memory device or memory module incorporating the same, for example, memory devices

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[4] The '459 Application suggests the use of "The latest dynamic RAMs" featuring "Nibble Mode Support" as in "*Nikkei Electronics,* April 1983." (see page 8, lines 38-39).

like those described in the Kung et al., U.S. Pat. 4,449,207, and Voss,

U.S. Pat. 4,646,270. The memory 1 described in the '459 Application

does not appear to input or output data synchronously with respect to

a clock signal. Instead, control signals such as function signal 241

and memory response signal 240, generated by memory control device 2,

are employed to signal the transfer of data between memory 1 and memory

control device 2. (See, the '459 Application, Figure 9, and page 7,

lines 26-34). The writing of data to memory 1 from memory control

device 2 is described on page 7, lines 31-34 as follows:

> ...after response 240 is acquired, if memory function signal
> 241 is made the write mode [ ] the contents of transfer
> destination address counter 203 are output as memory address
> signal 242, memory data 243 is transferred to and stored at
> the transfer destination memory area."

The '459 App. Does Not Anticipate Claims 151-153, 156, 159, 178, and 180

Claim 151 is directed to a method of controlling a memory device

and requires, among other things, providing first block size

information to the memory device. The first block size information is

representative of a first amount of data to be input by the memory

device in response to an operation code.

As mentioned above, information indicating the number of words to

be transferred by the memory control device 2 is not provided to memory

1. Instead, memory control device 2 of the '459 Application receives,

decodes and stores that information in a counter, and, based thereon,

Page 7

sequentially generates the address and control signals necessary to write the words to the memory device. In this regard, the system described in the '459 Application is similar to the system described in Jackson, U.S. Pat. 4,315,308[5]. The claims of the parent (i.e., App. Ser. No. 09/252,997, now, U.S. Pat. 6,034,918) of the instant application were initially rejected as being anticipated by Jackson but ultimately found patentable over Jackson.

Importantly, memory 1 of the '459 Application does not receive information indicating the number of words to be transferred. The memory 1 simply responds to the sequentially applied address and control signals provided by memory control device 2.

Thus, for at least these reasons, the '459 Application does not anticipate claim 151 or the claims which depend therefrom.[6]

The '459 App. Does Not Anticipate Claims 161, 162, and 166-167, and 182-184

Claim 161 is directed to a method of operation in a memory device, and, like claim 151, requires that the memory device receive first block size information from a memory controller.

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[5] Jackson, U.S. Patent 4,315,308, formed the basis of the 35 U.S.C. §102(b) rejection made in the parent application (App. Ser. No. 09/252,997, now, U.S. Patent 6,034,918) It was previously noted that the '459 Application is similar in many respects to Jackson.

[6] It should be noted that claim 152 requires that the memory device inputs the first amount of data synchronously with respect to an external clock signal. The memory disclosed in the '459 Application does not input data in this manner.

Page 8

For reasons similar to those mentioned above, the memory disclosed in the '459 Application does not receive the information indicating the number of words to be transferred. The memory of the '459 Application simply responds to the sequentially applied address and control signals from the memory control device 2. The memory control device 2 receives, decodes and stores information that indicates the number of words to be transferred to memory 1 in a counter, and, based thereon, generates and sequentially applies the appropriate address and control signals necessary to write the appropriate number of words to memory 1. The information indicating the number of words to be transferred is _not_ provided to memory 1.

Thus, for _at least_ these reasons, the '459 Application does not anticipate claim 161 or the claims which depend therefrom.

The '459 App. Does Not Anticipate Claims 171-172, 174 and 186

Claim 171 is directed to a method of operation of an integrated circuit, wherein the integrated circuit includes a dynamic random access memory array. Claim 171 requires, among other things, that the integrated circuit _receive_ block size information. The memory device disclosed in the '459 Application does _not_ receive the information indicating the number of words to transfer. Thus, for _at least_ this reason, the '459 Application does not anticipate claim 171 or its dependent claims.

Page 9

Information Disclosure Statement

Applicants submit concurrently herewith an Information Disclosure Statement (IDS) and accompanying Form PTO-1449, identifying two (2) references, namely U.S. Patent 5,034,964 and Japanese Patent Application No. S62-51509, that were both identified in previous IDS submissions, but were not clearly noted (by way of, for example, the Examiner's initials) by the Examiner as being formally considered. For the convenience of the Examiner, a copy of the Form PTO-1449 identifying each reference is attached. It is respectfully requested that the Examiner make his consideration of these references clearly and formally of record with the next Action.

CONCLUSION

Applicants request entry of the foregoing Amendment. Applicants submit that all of the claims present patentable subject matter. Accordingly, allowance of all of the claims is respectfully requested.

It is noted that should a telephone interview expedite the prosecution in any way, the Examiner is invited to contact Neil Steinberg at 650-947-5325.

Respectfully submitted,

Date: May 31, 2001

Neil A. Steinberg
Reg. No. 34,735
650-947-5325

Page 10

2&8

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
(Case No. P043D2C3C)

In the Application of:

   FARMWALD et al.

Serial No: 09/492,982

Filed: JANUARY 27, 2000

Title: METHOD OF OPERATING A MEMORY
     DEVICE HAVING A VARIABLE DATA
     INPUT LENGTH

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Group
Art Unit: 2818

Before
Examiner: T. Nguyen

Assistant Commissioner for Patents
Washington, DC 20231

INFORMATION DISCLOSURE STATEMENT

Dear Sir:

    Applicants submit concurrently herewith an Information Disclosure Statement (IDS) citation Form PTO-1449, listing 2 (two) references, namely U.S. Patent 5,034,964 (hereinafter the '964) and Japanese Patent Application No. 562-51509 (hereinafter the '509). Both the '964 and '509 have been identified in previous IDS submissions, but not noted (by way of, for example, the Examiner's initials) by the Examiner as being formally considered. For the convenience of the Examiner, a copy of the Form PTO-1449 identifying each reference is attached.

    It is respectfully requested that the Examiner make his consideration of these references formally of record with the next Action. The Commissioner is hereby authorized to charge Applicants' Deposit Account No. 50-0998 for any fee required in connection with this submission. A duplicate copy of this sheet is enclosed.

               Respectfully submitted,

Date: May 31, 2001

               Neil A. Steinberg
               Reg. No. 34,735
               650-947-5325

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
(Case No. P043D2C3C)

In the Application of:

FARMWALD et al.

COPY

Serial No: 09/492,982

Filed: JANUARY 27, 2000

Title: METHOD OF OPERATING A MEMORY
DEVICE HAVING A VARIABLE DATA
INPUT LENGTH

Group
Art Unit: 2816

Before
Examiner: T. Nguyen

I hereby certify that this correspondence is being
deposited with the United States Postal Service
as first class mail with sufficient postage in an
envelope addressed to the Commissioner of
Patents and Trademarks, Washington, D.C.
20231 on _____
(Name of Person Mailing Correspondence)

_____   _____
Signature   Date

Assistant Commissioner for Patents
Washington, DC 20231

INFORMATION DISCLOSURE STATEMENT

Dear Sir:

Applicants submit concurrently herewith an Information Disclosure Statement (IDS) citation Form PTO-1449, listing 2 (two) references, namely U.S. Patent 5,034,964 (hereinafter the '964) and Japanese Patent Application No. S62-51509 (hereinafter the '509). Both the '964 and '509 have been identified in previous IDS submissions, but not noted (by way of, for example, the Examiner's initials) by the Examiner as being formally considered. For the convenience of the Examiner, a copy of the Form PTO-1449 identifying each reference is attached.

It is respectfully requested that the Examiner make his consideration of these references formally of record with the next Action. The Commissioner is hereby authorized to charge Applicants' Deposit Account No. 50-0998 for any fee required in connection with this submission. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

Date: May 31, 2001

Neil A. Steinberg
Reg. No. 34,735
650-947-5325

	ATTY. DOCKET NO. P043D2C3C	SERIAL NUMBER 09/492,982
PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	APPLICANT(S) FARMWALD ET AL.	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	FILING DATE JANUARY 27, 2000	GROUP ART UNIT 2818

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
TNT	5,034,964	Jul. 23, 1991	Khan et al.	375	242	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO	
TNT	62-51509	Mar. 6, 1987	Japan	—	—	YES	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER TAN T. NGUYEN	DATE CONSIDERED 07/12/01

EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant.

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(54)   Name of Invention: Method for Setting Memory Access Timing

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Details

1.   Name of Invention
       Method for Setting Memory Access Timing

2.   Patent Claims

A method for setting memory access timing in a logical circuit that accesses memory, characterized by the provision of a register for which a variety of values can be set by a program, by repetitively having the value set in said register be changed sequentially by the program and performing test writes to the memory and test reads from the memory where the data that is written is compared to the data that is read, by setting to the register the setting that was in effect when the results of the comparison matched, and by accessing the memory based on said setting.

1.   Detailed Explanation of the Invention

[Area of Application in Industry]

This invention pertains to a method for setting the memory access timing in order to set the access timing for random access memory (hereinafter abbreviated "RAM") that is equipped in, for example, data processing devices.

[Prior Art]

Figure 6 shows a block diagram of the logic circuits that use the conventional memory access timing set method. In the figure, 1 is RAM (using the example where a dynamic RAM is used), 2 is an address multiplexer, 3 is a multiplexed address bus connecting the RAM 1 with the address multiplexer 2, 4 is an address bus connected to the address multiplexer 2, 5 is a data bus connected to the RAM 1, and 6 is a memory control ring. In addition, 7 is a flipflop for generating the row address select signal (RAS signal), hereinafter abbreviated "RAS flipflop," 8 is a flipflop for generating the column address select signal (CAS signal), hereinafter abbreviated "CAS flipflop," 9 is a flipflop for generating the column select signal (COLS signal), hereinafter abbreviated "COLS flipflop." 10 is an AND gate, 11, 12, and 13 are OR gates. 14, 15, and 16 are NOR gates, and 17, 18, 19, and 20 are jumper lines for selecting the output from the memory control ring 6 that is to be used. Additionally, for simplicity in the explanation, the logic circuits for refreshing the RAM 1 are not shown.

The operation of this method is described below. In this explanation, "1" indicates either the active level or the high logic level, while "0" indicates the inactive level or the low logic level. The memory control ring 6 is enabled and placed in an operational state when the memory access mode signal of line L1 goes to "1." and, synchronized to the master clock on line L2, the outputs T0, T1, . . . Tk, . . . Tl, . . . , Tm, . . ., Tn, . . ., Te-1, Te are sequentially set to "1" in the state transitions. When the memory access mode signal is "0," all outputs T0 to Te from the memory control ring 6 go to "0." The respective flipflops 7, 8, and 9 each output their latched signals from the output terminal 1 on each; and output the inverse of the latched signal on output terminal 0 of each. The RAS signal, CAS signal, and WE signal applied, respectively, to the RAS, CAS, and WE terminals of RAM 1 are each active at "1." In this conventional example, jumper lines 17, 18, 19, and 20 are set by hand, selecting, respectively, outputs Tk, Tl, Tm, and Tn of the memory control ring 6.

Below will be explained an example of an operation to write to the RAM 1, referencing the timing chart shown in Figure 4. When the memory access commences, both the memory access mode signal on Line L1 and the write mode signal on Line 3 both go to "1." At this time, the address is applied to the address bus 4, the row address is selected by the address multiplexer 2 and is output on the multiplexed address bus 3. At this time the write data is applied to data bus 5.

In this way, the row address and write data are applied, and, as described above, the memory access mode signal of line L1 is at "1," so the memory control ring 6 commences operations, and there are state transitions so that outputs T0, T1, ... Tk sequentially go to "1." When Tk goes to "1," the "1" output Tk is applied to terminal D of the RAS flipflop 7 through the jumper line 17 and OR gate 11, and when output Tk + 1 of memory control ring 6 goes to "1," the RAS signal that is output from output terminal 1 of the RAS flipflop 7 goes to "1." In addition, at this time the inverted signal that is output from the output terminal 0 of the RAS flipflop 7 goes to "0," causing the output of the NOR gate 14 to go to "1," and the output of the OR gate 11 to go to "1," causing the output of the RAS flipflop 7, or in other words the RAS signal, to be held at "1" even if the memory control ring 6 status advances. When the "1" output of the memory control ring 6 transitions from Tl to Tl + 1, the same operation as described above causes the COLS signal, which is the output of the COLS flipflop 9, to be held at "1." This COLS signal causes the address multiplexer 2 to output the column address to the multiplexed address bus 3, and the output of the AND gate 10, or in other words the WE signal that is applied to the RAM 1 terminal WE, goes to "1," placing RAM 1 in write mode. When the "1" output of the memory control ring 6 transitions from Tm to Tm + 1, a operation similar to what was described above causes the output of the CAS flipflop 8, or in other words the CAS signal, to be held at "1." As described above, the RAS signal, the CAS signal, the WE signal, and the COLS signal all go to "1," putting all conditions in place to write to the RAM 1; hence the data write operation is performed, the status of the memory control ring 6 advances, and the write operation is concluded at the point in time where the output Tn - 1 goes to "1." When the output Tn of the memory control ring 6, or in other words the memory access complete signal on line 4, goes to "1" followed by the output Tn + 1 going to "1," the memory access mode signal on line L1 and the write mode signal on line L3 both go to "0," causing the outputs of the NOR gates 14, 15, and 16, along with the outputs of the OR gates 11, 12, and 13 to go to "0"; consequently, the RAS signal, the CAS signal, and the COLS signal all go to "0," completing the operation for writing to the RAM 1. Note that TW shown in Figure 4 is the period over which the write mode conditions are fulfilled by the control signals to the RAM 1 (i.e., the memory access mode signal, the write mode signal, the RAS signal, the COLS signal, the CAS signal, and the WE signal).

On the other hand, in the operations to read from the RAM 1, as shown in Figure 5, the write mode signal and the WE signal go to "0," and at the point in time when the output Tn - 1 of the memory control ring 6 ceases to output "1," or in other words, at the point in time when the output Tn goes to "1," the output data that is read from the RAM 1 is assumed to be set, and with the output Tn, the data on the data bus 5 is accepted. At this time, when, in operations similar to the write operations described above the output Tn + 1 of the memory control ring 6 is to go to "1," all control signals become inactive and the operations to read from the

RAM 1 are terminated. Note that the TR shown in Figure 5 is the period of time over which the control signals to the RAM 1 fulfill the read mode conditions.

[Problems Solved by this Invention]

In the conventional method for setting the memory access timing, the part that sets the RAM access timing is set by jumper lines, and thus it requires a manual intervention to set the jumper lines. Additionally, generally RAMs have a variety of different access times, and when the type of RAM that is used is changed it is necessary to change the settings of the jumpers in order to change the access timing, and, as a result, the RAM cannot be accessed correctly if the setting is incorrect or there may also be the problem that, even if RAM that can operate at high speeds is used, the actual performance of the RAM will not be good if the access timing used is for low speed RAM.

This invention was created in order to solve the types of problems described above, and its objective is to provide a method of setting the memory access timing that automatically sets the access timing without any manual intervention, making it possible to exploit the full capabilities of the RAM and to improve reliability.

[Method by Which the Problems are Solved]

The method of setting the memory access timing in this invention is characterized by the logic circuits that access the memory (RAM 1) being equipped with registers 21, 22, 23, and 24 that can be set to a variety of values by a program, where the values that are set to these registers 21, 22, 23, and 24 are repetitively changed sequentially by the program at which time test data is written to and read from the memory (RAM 1) and comparisons are made between the write data and the read data where the values that were set when the results of the comparison indicates a match are set to registers 21, 22, 23, and 24, so that the access to the memory (RAM 1) is performed based on these settings.

[Operation]

The registers 21, 22, 23, and 24 in this invention are set to any given value by the program, and the memory (RAM 1) is accessed based on the various settings that have been set, at which time test data is written to the memory and read from the memory. The data written as this test data, and the data that is read, are compared to each other for each of the access operations that are based on the respective settings, and when the data that is written to the memory (RAM 1) matches the data that is read from the memory, then the settings are set as the final settings in the registers 21, 22, 23, and 24, and after that time the access timing is determined based on these final settings and the memory (RAM 1) is accessed with that access timing when the specific data write and data read operations are performed.

[Example of Embodiment]

An Example of Embodiment of this invention is explained below based on the figures. Figure 1 is a block diagram of logic circuits that use the method for setting the memory access timing in this Embodiment of the invention. In Figure 1 the same symbols are used as corresponding to the structural elements shown in Figure 6, so the explanations are omitted here. In Figure 1, 21 is the register for determining the timing with which the RAS signal is produced (hereinafter termed the "RAS register"), 22 is the register for determining the timing with which the COLS signal is produced (hereinafter termed the "COLS register"), 23 is the register for determining the timing with which the CAS signal is produced (hereinafter termed the "CAS register"), 24 is the register for determining the timing with which the memory access complete signal will be produced (hereinafter termed the "CPLT register"), 25, 26, 27, and 28 are the selectors that select one output from output T0 to Te of the e + 1 registers in memory control ring 6.

Next the operation will be explained. Let us assume that there are five different types of RAM that can be obtained, and, the access timing on these types of RAM, from fastest to slowest, are RAM_1, RAM_2, RAM_3 RAM_4, and RAM_5. The respective RAMs can be accessed correctly by outputting the RAS signals, COLS signals, CAS signals, and memory access complete signals shown in the timing diagram of Figure 2. The explanation described below considers the operations when RAM_2 is installed.

The table has the settings for the RAS register 21, the COLS register 22, the CAS register 23, and the CPLT register 24, or in other words, the settings for k1 to k5, l1 to l5, m1 to m5, and n1 to n5 in Figure 2, are stored as a table. This program executes the flow chart shown in Figure 3. In other words, the program is executed (Step S1), the pointer indicates RAM_1 (Step S2), the information indicated by the pointer (in this case, the settings k1 corresponding to RAM_1 shown in Figure 2) are loaded into RAS register 21 (Step S3), the pointer is then incremented (Step S4), the information indicated by the pointer (in this case, the setting l1 corresponding to RAM_1) is loaded into the COLS register 22 (Step S5), the pointer is incremented (Step S6), the information indicated by the pointer (in this case, the setting m1 corresponding to RAM_1) is loaded into the CAS register 23 (Step S7), the pointer is incremented (Step S8), the information indicated by the pointer (in this case the setting n1 corresponding to RAM_1) is loaded into the CPLT register 24 (Step S9), the pointer is incremented (Step S10), the test data is written into the RAM_2 (because in this case it is RAM_2 that is installed) (Step S11), and the write operation is performed with the timing shown in Figure 4. Then the data is read from the RAM_2 with the timing shown in Figure 5 (Step S12), and the data that was read is compared to the data that was written (Step S13). In this case, the settings are the settings k1, l1, m1, and n1 that correspond to RAM_1. These settings do not match the timing for the control signals (the RAS signal, the COLS signal, the CAS signal, and the memory access complete signal) for RAM_2, so the comparison in Step 13 of the data that was read and the data that

was written does not indicate a match with this timing. As a result, the program continues to Step S14, and a check is made for a pointer error. If there is an error then an error report is made (Step S15), and if there is no error, then the program returns to Step S3.

The information indicated by the pointer when the program returns to Step S3 is the setting k2 that corresponds to the RAM$_2$ that is installed, and this setting k2 is loaded into the RAS register 21. After that, the same process that is described above is performed (Steps S4 through S10) and the setting l2 is loaded into the COLS register 22, the setting m2 is loaded into the CAS register 23, the setting n2 is loaded into the CPLT register 24, the test data is written to the RAM$_2$ (Step S11) the data is read from the RAM$_2$ (Step S12), and the data that was written is compared to the data that was read (Step 13). In this case, the RAM access timing is set so that, when the operations for writing and reading the specified data are performed, the settings k2, l2, m2, and n2 correspond to RAM$_2$, and thus RAM$_2$ is accessed with the appropriate timing and the data that was read matches the data that was written so the program continues to Step 16 and the settings k2, g2, m2, and n2 are set into registers 21, 22, 23, and 24 as the final settings, and selectors 25, 26, 27, and 28 cause the RAS signal to be "1" when the output Tk2 + 1 of the memory control ring 6 is "1," the COLS signal to be "1" when the output Tl2 + 1 is "1," the CAS signal to be "1" when the output Tm2 + 1 is "1," and the memory access complete signal to be "1" when the output Tn2 is "1." In addition, when the output Tn2 + 1 is "1" the RAS signal, the COLS signal, the CAS signal and the memory access complete signal all go to "0."

While the explanation of the flow chart was based on the assumption that RAM 2 was installed, if RAM$_1$, RAM$_3$, RAM$_4$, or RAM$_5$ were installed instead, the processes in Steps 3 through 13 would be performed once, three times, four times, or five times, respectively, to set the access timing.

Because in the Example of Embodiment described above, it is possible to change the access timing using a program, it is easy to perform RAM access timing margin tests. In addition, although the timing will be that for the type of RAM with the slowest access time, even if a mixture of RAMs with different access times are installed in the logic circuits, the RAM can still be accessed correctly. In addition, if in high-speed computers, the RAM access timing is set individually by the card unit or the bank unit of main memory, then even if the type of RAM is different on different card units or bank units, the timing can be performed to match the capability of the RAM, making it possible to prevent any impediments to performance by mixing types of RAM. Additionally, in the program that determines the settings, it is possible to set the access timing that is optimized for the RAM that is installed and that is able to fully exploit the capabilities of the RAM through selecting the optimal values through changing the settings in even finer increments, rather than determining the settings in such a way as to compensate for the minor timing differences between the various RAM manufacturing locations. If in the program access timing setting checks are

performed for all addresses of all RAM, then it is possible to identify the RAM that has errors even if different types of RAM (with different access times) are mixed.

Furthermore, in the Example of Embodiment described above, dynamic RAM was used as the example. when static RAM is used then the chip select (CS) signal and the output enable (OE) signal can be controlled instead of the RAS signal and the CAS signal. Although in the Example of Embodiment above a memory control ring was used to control the RAM access timing, the method of this invention can also be performed by establishing for each signal to be controlled by the program a combination of a counter into which data can be loaded and a register that sets the value that is loaded into the counter as the initial value.

(Effects of the Invention)

Using the invention described above, it is possible to set the memory access timing automatically without a manual intervention because a register is provided wherein a variety of different values can be set by the program where the values that are set into this register are repetitively changed sequentially, test data is written to the memory and then read from the memory. and the data that was written is compared to the data that is read and the values that were set when the results of the comparison indicate a match are set to the register so that the memory is accessed based on those settings. it is able to prevent any disruptions to memory performance or situations where access cannot be performed normally due to incorrect settings in the access timing, making it possible to fully exploit the capabilities of the memory, and thus possible to obtain the effect of increased reliability; in addition. it is no longer necessary to have a manual intervention in order to set the access timing using jumper lines as it has been conventionally, thus making it possible to reduce operating test expenses and reduce labor expenses, and making it possible to provide data processing equipment less expensively.

4.   Simple Explanation of Figures

Figure 1 is a block diagram of the logic circuits that use the method for setting the memory access timing in the Example of Embodiment of this invention.
Figure 2 is a timing diagram showing the relationship between the settings and the access timing in this Example of Embodiment.
Figure 3 is a flow chart used for explaining the operation of the Example of Embodiment.
Figure 4 is a timing chart for explaining a conventional example and explaining the operations for writing to the RAM in the Example of Embodiment thereof.
Figure 5 is a timing chart for explaining the conventional example and for explaining the operations for reading from the RAM in an example thereof.
Figure 6 is a block diagram of the logic circuits that use the conventional method of setting the memory access timing.

1:      RAM (memory)
2:      Address multiplexer
6:      Memory control ring
7:      RAS flipflop
8:      CAS flipflop
9:      COLS flipflop
10:     AND gate
11, 12, 13:   OR gates
14, 15, 16:   NOR gates
21:     RAS register
22:     COLS register
23:     CAS register
24:     CPLT register
25, 26, 27, 28: Selectors

Representative: Masao Oiwa, and two others

Figure 1
[L1]   Memory access mode signal
[L2]   Fundamental clock
[6]   Memory control ring
[21]   Register
[25]   Selector
[22]   Register
[26]   Selector
[23]   Register
[27]   Selector
[24]   Register
[28]   Selector
[L4]   Memory access complete signal
[Under 14]   RAS signal
                CAS signal
[2]   Address multiplexer
[Above 10]   COLS signal
[L3]   Write mode signal

Figure 2
[INSERT TABLE]

Type of RAM	RAS signal timing	COLS signal timing	CAS signal timing	Memory access comple to signal timing	Settings for the registers for generating the timing			
					Registe	Registe	Registe	Registe

					r 21	r 22	r 23	r 24
(see source for English)								

Figure 3
S1   Start
S2   Set pointer = PRAM 1
S3   Load the information indicated by the pointer into the RAS register
S4   Pointer = pointer + 1
S5   Load the information indicated by the pointer into the COLS register
S6   Pointer = pointer + 1
S7   Load the information indicated by the pointer into the CAS register
S8   Pointer = pointer + 1
S9   Load the information indicated by the pointer into the CPLT register
S10   Pointer = pointer + 1
S11   Write test data to the RAM
S12   Read test data from the RAM
S13   Compare the read data to the write data
S14   Is there a pointer error?
S15   Error report
S16   Settings complete

Figure 4
Fundamental clock
Memory access mode signal
Write mode signal
T0
T1
Tk
Te
Tm
Tn (Memory access complete signal)
RAS signal
COLS signal
CAS signal
WE signal

Figure 5
Fundamental clock
Memory access mode signal
Write mode signal
T0
T1
Tk
Te
Tm
Tn (Memory access complete signal)

RAS signal
COLS signal
CAS signal
WE signal

Figure 6
[L1]   Memory access mode signal
[L2]   Fundamental clock
[6]   Memory control ring
[L4]   Memory access complete signal
[Under L4]   RAS signal
                     CAS signal
                     WE signal
[2]   Address multiplexer
[Above 10]   COLS signal
[L3]   Write mode signal

APPLICATION NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.
09/492,982	01/27/00	FARMWALD	M P043D2C3C

EXAMINER

MM41/0716

NGUYEN T

ART UNIT	PAPER NUMBER
2818	25

NEIL A STEINBERG ESQ
RAMBUS INC
4440 EL CAMINO REAL
LOS ALTOS CA 94022

DATE MAILED:
07/16/01

This is a communication from the examiner in charge of this application.
COMMISSIONER OF PATENTS AND TRADEMARKS

NOTICE OF ALLOWABILITY

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance and Issue Fee Due or other appropriate communication will be mailed in due course. THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS. This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

☑ This communication is responsive to *the Response filed on 06/01/01*

☑ The allowed claim(s) is/are *151 - 174 and 176 - 186*

☐ The drawings filed on _____ are acceptable as formal drawings.

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

☐ All ☐ Some* ☐ None of the:
  ☐ Certified copies of the priority documents have been received.
  ☐ Certified copies of the priority documents have been received in Application No. _____
  ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with requirements noted below. Failure to timely comply will result in ABANDONMENT of this application. THIS THREE-MONTH PERIOD IS NOT EXTENDABLE FOR SUBMITTING NEW FORMAL DRAWINGS, OR A SUBSTITUTE OATH OR DECLARATION. This three-month period for complying with the REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL is extendable under 37 CFR 1.136(a).

☐ Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL APPLICATION, PTO-152, which discloses that the oath or declaration is deficient. A SUBSTITUTE OATH OR DECLARATION IS REQUIRED.

☑ Applicant MUST submit NEW FORMAL DRAWINGS

☐ because the originally filed drawings were declared by applicant to be informal.

☑ including changes required by the Notice of Draftperson's Patent Drawing Review, PTO-948, attached hereto or to Paper No. *25*

☐ including changes required by the proposed drawing correction filed on _____, which has been approved by the examiner.

☐ including changes required by the attached Examiner's Amendment/Comment or in the Office action of Paper No. _____

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings.

☐ Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Any reply to this notice should include, in the upper right hand corner, the APPLICATION NUMBER (SERIES CODE/SERIAL NUMBER). If applicant has received a Notice of Allowance and Issue Fee Due, the ISSUE BATCH NUMBER and DATE of the NOTICE OF ALLOWANCE should also be included.

Attachment(s)
☐ Notice of References Cited, PTO-892
☑ Information Disclosure Statement(s), PTO-1449, Paper No(s). *24*
☑ Notice of Draftsperson's Patent Drawing Review, PTO-948
☐ Notice of Informal Patent Application, PTO-152
☐ Interview Summary, PTO-413
☐ Examiner's Amendment/Comment
☐ Examiner's Comment Regarding Requirement for the Deposit of Biological Material
☐ Examiner's Statement of Reasons for Allowance

TAN T. NGUYEN
PRIMARY EXAMINER
GROUP 2800

PTOL-37 (Rev 11/00)

NOTICE OF DRAFTSPERSON'S
PATENT DRAWING REVIEW

The drawing(s) filed (insert date) 12/18/00 are:

A.☐ approved by the Draftsperson under 37 CFR 1.84 or 1.152.
B.☑ objected to by the Draftsperson under 37 CFR 1.84 or 1.152 for the reasons indicated below. The Examiner will require submission of new, corrected drawings when necessary. Corrected drawing must be submitted according to the instructions on the back of this notice.

1. DRAWINGS. 37 CFR 1.84(a): Acceptable categories of drawings:
   Black Ink. Color.
   ___ Color drawings are not acceptable until petition is granted.
   Fig(s)_____
   ___ Pencil and non black ink not permitted. Fig(s)_____
2. PHOTOGRAPHS. 37 CFR 1.84(b)
   ___ 1 full-tone set is required. Fig(s)_____
   ___ Photographs may not be mounted. 37 CFR 1.84(e)
   ___ Poor quality (half-tone). Fig(s)_____
3. TYPE OF PAPER. 37 CFR 1.84(e)
   ___ Paper not flexible, strong, white, and durable.
   Fig(s)_____
   ___ Erasures, alterations, overwritings, interlineations, folds, copy machine marks not accepted. Fig(s) 1-4
   ___ Mylar, velum paper is not acceptable (too thin).
   Fig(s)_____
4. SIZE OF PAPER. 37 CFR 1.84(f): Acceptable sizes:
   ___ 21.0 cm by 29.7 cm (DIN size A4)
   ___ 21.6 cm by 27.9 cm (8 1/2 x 11 inches)
   ___ All drawing sheets not the same size.
   Sheet(s)_____
   ___ Drawings sheets not an acceptable size. Fig(s)_____
5. MARGINS. 37 CFR 1.84(g): Acceptable margins:
   Top 2.5 cm Left 2.5 cm Right 1.5 cm Bottom 1.0 cm
   SIZE: A4 Size
   Top 2.5 cm Left 2.5 cm Right 1.5 cm Bottom 1.0 cm
   SIZE: 8 1/2 x 11
   ___ Margins not acceptable. Fig(s) 4,5,15
   ___ Top (T) ___ Left (L)
   ___ Right (R) ___ Bottom (B)
6. VIEWS. 37 CFR 1.84(h)
   REMINDER: Specification may require revision to correspond to drawing changes.
   Partial views. 37 CFR 1.84(h)(2)
   ___ Brackets needed to show figure as one entity.
   Fig(s)_____
   ___ Views not labeled separately or properly.
   Fig(s)_____
   ___ Enlarged view not labeled separately or properly.
   Fig(s)_____
7. SECTIONAL VIEWS. 37 CFR 1.84 (h)(3)
   ___ Hatching not indicated for sectional portions of an object.
   Fig(s)_____
   ___ Sectional designation should be noted with Arabic or Roman numbers. Fig(s)_____

8. ARRANGEMENT OF VIEWS. 37 CFR 1.84(i)
   ___ Words do not appear on a horizontal, left-to-right fashion when page is either upright or turned so that the top becomes the right side, except for graphs. Fig(s)_____
9. SCALE. 37 CFR 1.84(k)
   ___ Scale not large enough to show mechanism without crowding when drawing is reduced in size to two-thirds in reproduction.
   Fig(s)_____
10. CHARACTER OF LINES, NUMBERS, & LETTERS.
    37 CFR 1.84(l)
    ___ Lines, numbers & letters not uniformly thick and well defined, clean, durable, and black (poor line quality).
    Fig(s)_____
11. SHADING. 37 CFR 1.84(m)
    ___ Solid black areas pale. Fig(s)_____
    ___ Solid black shading not permitted. Fig(s)_____
    ___ Shade lines, pale, rough and blurred. Fig(s)_____
12. NUMBERS, LETTERS, & REFERENCE CHARACTERS.
    37 CFR 1.84(p)
    ___ Numbers and reference characters not plain and legible.
    Fig(s)_____
    ___ Figure legends are poor. Fig(s)_____
    ___ Numbers and reference characters not oriented in the same direction as the view. 37 CFR 1.84(p)(1)
    Fig(s)_____
    ___ English alphabet are used. 37 CFR 1.84(p)(2)
    Figs_____
    ___ Numbers, letters and reference characters must be at least .32 cm (1/8 inch) in height. 37 CFR 1.84(p)(3)
    Fig(s)_____
13. LEAD LINES. 37 CFR 1.84(q)
    ___ Lead lines cross each other. Fig(s)_____
    ___ Lead lines missing. Fig(s)_____
14. NUMBERING OF SHEETS OF DRAWINGS. 37 CFR 1.84(t)
    ___ Sheets not numbered consecutively, and in Arabic numerals beginning with number 1. Sheet(s)_____
15. NUMBERING OF VIEWS. 37 CFR 1.84(u)
    ___ Views not numbered consecutively, and in Arabic numerals, beginning with number 1. Fig(s)_____
16. CORRECTIONS. 37 CFR 1.84(w)
    ___ Corrections not made from prior PTO-948 dated_____
17. DESIGN DRAWINGS. 37 CFR 1.152
    ___ Surface shading shown not appropriate. Fig(s)_____
    ___ Solid black shading not used for color contrast.
    Fig(s)_____

COMMENTS

REVIEWER _____ DATE 7/13/01 TELEPHONE NO. 308-001

ATTACHMENT TO PAPER NO. 25

Attachment for PTO-948 (Rev. 03/01, or earlier)
6/18/01

The below text replaces the pre-printed text under the heading,
"Information on How to Effect Drawing Changes," on the back
of the PTO-948 (Rev. 03/01, or earlier) form.

INFORMATION ON HOW TO EFFECT DRAWING CHANGES

1. Correction of Informalities – 37 CFR 1.85

New corrected drawings must be filed with the changes incorporated therein.
Identifying indicia, if provided, should include the title of the invention,
inventor's name, and application number, or docket number (if any) if an
application number has not been assigned to the application. If this information is
provided, it must be placed on the front of each sheet and centered within the top
margin. If corrected drawings are required in a Notice of Allowability (PTOL-
37), the new drawings MUST be filed within the THREE MONTH shortened
statutory period set for reply in the Notice of Allowability. Extensions of time
may NOT be obtained under the provisions of 37 CFR 1.136(a) or (b) for filing
the corrected drawings after the mailing of a Notice of Allowability. The
drawings should be filed as a separate paper with a transmittal letter addressed to
the Official Draftsperson.

2. Corrections other than Informalities Noted by Draftsperson on form PTO-
948.

All changes to the drawings, other than informalities noted by the Draftsperson,
MUST be made in the same manner as above except that, normally, a highlighted
(preferably red ink) sketch of the changes to be incorporated into the new
drawings MUST be approved by the examiner before the application will be
allowed. No changes will be permitted to be made, other than correction of
informalities, unless the examiner has approved the proposed changes.

Timing of Corrections

Applicant is required to submit the drawing corrections within the
time period set in the attached Office communication. See 37 CFR
1.85(a).

Failure to take corrective action within the set period will result in
ABANDONMENT of the application.

06/01/01

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office

NOTICE OF ALLOWANCE AND ISSUE FEE DUE

NM41 /07/16

NEIL A STEINBERG ESQ
RAMBUS INC
4440 EL CAMINO REAL
LOS ALTOS CA 94022

APPLICATION NO.	FILING DATE	TOTAL CLAIMS	EXAMINER AND GROUP ART UNIT		DATE MAILED
09/492,982	01/27/00	035	NGUYEN, T.	2818	07/16/0

First Named Applicant	FARMWALD.		35 USC 154(b) term ext. =	0 Days.	

TITLE OF INVENTION	METHOD OF OPERATING A MEMORY DEVICE HAVING A VARIABLE DATA INPUT LENGTH

ATTY'S DOCKET NO.	CLASS-SUBCLASS	BATCH NO.	APPLN. TYPE	SMALL ENTITY	FEE DUE	DATE DUE
3	P043D2P030	365-233.000	T11	UTILITY	NO	$1240.00	10/16/0

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT.
PROSECUTION ON THE MERITS IS CLOSED.

THE ISSUE FEE MUST BE PAID WITHIN _THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE_ OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. _THIS STATUTORY PERIOD CANNOT BE EXTENDED._

HOW TO RESPOND TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.
If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is changed, pay twice the amount of the FEE DUE shown above and notify the Patent and Trademark Office of the change in status, or
B. If the status is the same, pay the FEE DUE shown above.

If the SMALL ENTITY is shown as NO:

A. Pay FEE DUE shown above, or

B. File verified statement of Small Entity Status before, or with, payment of 1/2 the FEE DUE shown above.

II. Part B-Issue Fee Transmittal should be completed and returned to the Patent and Trademark Office (PTO) with your ISSUE FEE. Even if the ISSUE FEE has already been paid by charge to deposit account, Part B Issue Fee Transmittal should be completed and returned. If you are charging the ISSUE FEE to your deposit account, section "4b" of Part B-Issue Fee Transmittal should be completed and an extra copy of the form should be submitted.

III. All communications regarding this application must give application number and batch number.
Please direct all communications prior to issuance to Box ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: *Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.*

PATENT AND TRADEMARK OFFICE COPY

PTOL-85 (REV. 10-96) Approved for use through 06/30/95: (0651-0033)

09/492982

09/492.982	01/27/00	FARMWALD	
APPLICATION NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

MM41/0807

NEIL A STEINBERG ESQ
RAMBUS INC
4440 EL CAMINO REAL
LOS ALTOS CA 94022

NGUYEN, T.
EXAMINER

ART UNIT	PAPER NUMBER

09/18/01

DATE MAILED:

This is a communication from the examiner in charge of this application.
COMMISSIONER OF PATENTS AND TRADEMARKS *SUPPLEMENTAL*

NOTICE OF ALLOWABILITY

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or have previously mailed), a Notice of Allowance and Issue Fee Due or other appropriate communication will be mailed in due course. THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS. This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

☐ This communication is responsive to _____

☑ The allowed claim(s) is/are _151-174 and 176-186_

☐ The drawings filed on _____ are acceptable as formal drawings.

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

  ☐ All ☐ Some* ☐ None of the:

    ☐ Certified copies of the priority documents have been received.
    ☐ Certified copies of the priority documents have been received in Application No. _____
    ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

  *Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with requirements noted below. Failure to timely comply will result in ABANDONMENT of this application. THIS THREE-MONTH PERIOD IS NOT EXTENDABLE FOR SUBMITTING NEW FORMAL DRAWINGS, OR A SUBSTITUTE OATH OR DECLARATION. This three-month period for complying with the REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL is extendable under 37 CFR 1.136(a).

☐ Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL APPLICATION, PTO-152, which discloses that the oath or declaration is deficient. A SUBSTITUTE OATH OR DECLARATION IS REQUIRED.

☑ Applicant MUST submit NEW FORMAL DRAWINGS

☐ because the originally filed drawings were declared by applicant to be informal.

☑ including changes required by the Notice of Draftperson's Patent Drawing Review, PTO-948, attached hereto or to Paper No. _26_

☐ including changes required by the proposed drawing correction filed on _____, which has been approved by the examiner.

☐ including changes required by the attached Examiner's Amendment/Comment or in the Office action of Paper No. ____

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings.

☐ Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Any reply to this notice should include, in the upper right hand corner, the APPLICATION NUMBER (SERIES CODE/SERIAL NUMBER). If applicant has received a Notice of Allowance and Issue Fee Due, the ISSUE BATCH NUMBER and DATE of the NOTICE OF ALLOWANCE should also be included.

Attachment(s)

☐ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☑ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

☐ Interview Summary, PTO-413

☐ Examiner's Amendment/Comment

☐ Examiner's Comment Regarding Requirement for the Deposit of Biological Material

☐ Examiner's Statement of Reasons for Allowance

PTOL-37 (rev. 11/00)

TAN T. NGUYEN
PRIMARY EXAMINER
GROUP 2800

863 FH PG 0501

NOTICE OF DRAFTSPERSON'S
PATENT DRAWING REVIEW

The drawing(s) filed (insert date) 12/1/00 are:

A. ☐ approved by the Draftsperson under 37 CFR 1.84 or 1.152.
B. ☒ objected to by the Draftsperson under 37 CFR 1.84 or 1.152 for the reasons indicated below. The Examiner will require submission of new, corrected drawings when necessary. Corrected drawing must be submitted according to the instructions on the back of this notice.

1. DRAWINGS. 37 CFR 1.84(a): Acceptable categories of drawings:
   Black ink. Color.
   ___ Color drawings are not acceptable until petition is granted.
   Fig(s) _____
   ___ Pencil and non black ink not permitted. Fig(s) _____
2. PHOTOGRAPHS. 37 CFR 1.84(b)
   ___ 1 full-tone set is required. Fig(s) _____
   ___ Photographs may not be mounted. 37 CFR 1.84(e)
   ___ Poor quality (half-tone). Fig(s) _____
3. TYPE OF PAPER. 37 CFR 1.84(e)
   ___ Paper not flexible, strong, white, and durable.
   Fig(s) _____
   X Erasures, alterations, overwritings, interlineations, folds, copy machine marks not accepted. Fig(s) 1-15
   ___ Mylar, velom paper is not acceptable (too thin).
   Fig(s) _____
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   ___ 21.6 cm by 27.9 cm (8 1/2 x 11 inches)
   ___ All drawing sheets not the same size.
   Sheet(s) _____
   ___ Drawings sheets not an acceptable size. Fig(s) _____
5. MARGINS. 37 CFR 1.84(g): Acceptable margins:
   Top 2.5 cm Left 2.5 cm Right 1.5 cm Bottom 1.0 cm
   SIZE: A4 Size
   Top 2.5 cm Left 2.5 cm Right 1.5 cm Bottom 1.0 cm
   SIZE: 8 1/2 x 11
   Margins not acceptable. Fig(s) 4-6,15
   ___ Top (T) ___ Left (L)
   X Right (R) ___ Bottom (B)
6. VIEWS. 37 CFR 1.84(h)
   REMINDER: Specification may require revision to correspond to drawing changes.
   Partial views. 37 CFR 1.84 (h)(2)
   ___ Brackets needed to show figure as one entity.
   Fig(s) _____
   ___ Views not labeled separately or properly.
   Fig(s) _____
   ___ Enlarged view not labeled separately or properly.
   Fig(s) _____
7. SECTIONAL VIEWS. 37 CFR 1.84 (h)(3)
   ___ Hatching not indicated for sectional portions of an object.
   Fig(s) _____
   ___ Sectional designation should be noted with Arabic or Roman numbers. Fig(s) _____

8. ARRANGEMENT OF VIEWS. 37 CFR 1.84(i)
   ___ Words do not appear on a horizontal, left-to-right fashion when page is either upright or turned so that the top becomes the right side, except for graphs. Fig(s) _____
9. SCALE. 37 CFR 1.84(k)
   ___ Scale not large enough to show mechanism without crowding when drawing is reduced in size to two-thirds in reproduction.
   Fig(s) _____
10. CHARACTER OF LINES, NUMBERS, & LETTERS.
    37 CFR 1.84(l)
    ___ Lines, numbers & letters not uniformly thick and well defined, clean, durable, and black (poor line quality).
    Fig(s) _____
11. SHADING. 37 CFR 1.84(m)
    ___ Solid black areas pale. Fig(s) _____
    ___ Solid black shading not permitted. Fig(s) _____
    ___ Shade lines, pale, rough and blurred. Fig(s) _____
12. NUMBERS, LETTERS, & REFERENCE CHARACTERS.
    37 CFR 1.84(p)
    ___ Numbers and reference characters not plain and legible.
    Fig(s) _____
    ___ Figure legends are poor. Fig(s) _____
    ___ Numbers and reference characters not oriented in the same direction as the view. 37 CFR 1.84(p)(1)
    Fig(s) _____
    ___ English alphabet not used. 37 CFR 1.84(p)(2)
    Figs _____
    ___ Numbers, letters and reference characters must be at least .32 cm (1/8 inch) in height. 37 CFR 1.84(p)(3)
    Fig(s) _____
13. LEAD LINES. 37 CFR 1.84(q)
    ___ Lead lines cross each other. Fig(s) _____
    ___ Lead lines missing. Fig(s) _____
14. NUMBERING OF SHEETS OF DRAWINGS. 37 CFR 1.84(t)
    ___ Sheets not numbered consecutively, and in Arabic numerals beginning with number 1. Sheet(s) _____
15. NUMBERING OF VIEWS. 37 CFR 1.84(u)
    ___ Views not numbered consecutively, and in Arabic numerals, beginning with number 1. Fig(s) _____
16. CORRECTIONS. 37 CFR 1.84(w)
    ___ Corrections not made from prior PTO-948 dated _____
17. DESIGN DRAWINGS. 37 CFR 1.152
    ___ Surface shading shown not appropriate. Fig(s) _____
    ___ Solid black shading not used for color contrast.
    Fig(s) _____

COMMENTS

REVIEWER _____ DATE 8/3/01 TELEPHONE NO. 308-0011

ATTACHMENT TO PAPER NO. 26

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
(Case No. RA043D2C3C2)

In re Application of:)
)
        FARMWALD ET AL.   )
)
Serial No: Continuation of 09/492,982   )
)
Filed: Herewith   )
)
Title: MEMORY DEVICE HAVING A VARIABLE   )
           DATA OUTPUT LENGTH (As Amended)   )

Assistant Commissioner for Patents
Washington, DC 20231

REQUEST TO APPROVE DRAWING CHANGES

Dear Sir:

Attached hereto is new Figure 16. Figure 16 illustrates the internal registers which reside in each device illustrated in Figure 2. This embodiment is described in the specification at page 14, lines 3-21 and page 53 lines 4-21. No new matter has been added.

Applicants seek to amend Figure 10 to more fully reflect the discussion in the specification, specifically, page 55, line 12-16 and page 58, lines 13-23. Also attached is a photocopy of Figure 10 with the proposed changes indicated in red. No new matter has been added.

Applicants respectfully request that the proposed new Figure 16 be approved by the Examiner. Applicants also respectfully request approval of the proposed changes to Figure 10. A new Figure 10 which incorporates the changes is also attached hereto.

Respectfully submitted,

Date: _____Feb 7_____, 2001

Neil A. Steinberg
Reg. No. 34,735
650-947-5325

PATENTEC®
FILES

DUPLICATE ENTRY IN
U.S. PATENT OFFICE FILE WRAPPER
TABLE OF CONTENTS

PAPER 28 AND PAPER 31 FORMAL DRAWING

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
(Case No. P043D2C3C)

In the Application of:)
)
    FARMWALD et al.   )
)
Serial No: 09/492,982   )   Group
)   Art Unit: 2818   29/JDS
Filed: JANUARY 27, 2000   )
)   Before
)   Examiner: T. Nguyen
Title: METHOD OF OPERATING A MEMORY   )
         DEVICE HAVING A VARIABLE DATA   )
         INPUT LENGTH   )

Assistant Commissioner for Patents
Washington, DC 20231

INFORMATION DISCLOSURE STATEMENT

Dear Sir:

In compliance with the duty of disclosure set forth in 37 C.F.R.
§1.56, submitted herewith is a modified Form PTO-1449, including a copy
of all of the documents listed therein.

The documents listed in the PTO-1449 have been recently identified
in a Notice of Opposition filed against European Patent EP 1 004 956
(Hereinafter the "OPPOSITION"). EP 1 004 956 contains claims that are
similar to claims in U.S. Patent 6,034,918, the parent of the instant
application. A copy of the OPPOSITION is also submitted herewith.

It is respectfully requested that the Examiner make his
consideration of these references formally of record with the next
Action.

                              Respectfully submitted,

Date: January 29, 2001

                              Neil A. Steinberg
                              Reg. No. 34,735
                              650-947-5325

PTO-1449 (Modified)		ATTY. DOCKET NO. P043D2C3C		SERIAL NUMBER 09/492,982	
U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		APPLICANT(S) FARMWALD ET AL.			
INFORMATION DISCLOSURE STATEMENT BY APPLICANT		FILING DATE JANUARY 27, 2000		GROUP ART UNIT 2818	

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
TNT	4,763,249	08/09/88	Bomba et al	364	200	
T	4,394,753	07/19/83	Penzel	365	236	
	4,785,428	11/15/88	Bajwa	365	233	
TNT	4,680,738	07/14/87	Tam	365	239	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER TAN T. NGUYEN	DATE CONSIDERED 11/08/01

EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered.
Include copy of this form with next communication to applicant.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
(Case No. RA043D2C3C)

In the Application of:	)
	)
FARMWALD et al.	)
	) Group
Serial No: 09/492,982	) Art Unit: 2818
	)
Filed: JANUARY 27, 2000	) Before
	) Examiner: T. Nguyen
Title: METHOD OF OPERATING A MEMORY	)
DEVICE HAVING A VARIABLE DATA	)
INPUT LENGTH	)

Assistant Commissioner for Patents
Washington, DC 20231

Certificate of Mailing Under 37 CFR 1.8

I hereby certify that the attached 1) Information Disclosure Statement (2

pages) ; and 2) A Copy of a Petition under 37 CFR 1.313(b) (5) for Withdrawal From

Issue So That Information Can Be Considered in an Information Disclosure Statement

(2 pages) is/are being deposited with the United States Postal Service with sufficient

postage as first class U.S. mail in an envelope addressed to:

Assistant Commissioner for Patents
Washington, D.C. 20231

On January 30, 2001.

_____
(Signature)

Michiko Sites

(Print Name of Person Signing Certificate)

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 07-01)

APPLICATION NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.

EXAMINER

ART UNIT	PAPER NUMBER
	30

DATE MAILED:

This is a communication from the examiner in charge of this application.
COMMISSIONER OF PATENTS AND TRADEMARKS

SUPPLEMENTAL
NOTICE OF ALLOWABILITY

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance and Issue Fee Due or other appropriate communication will be mailed in due course. THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS. This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

☑ This communication is responsive to _the IDS filed on 02/02/01_.

☑ The allowed claim(s) is/are _151 - 186_.

☑ The drawings filed on _02/02/01_ are acceptable as formal drawings.

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

☐ All ☐ Some* ☐ None of the:
  ☐ Certified copies of the priority documents have been received.
  ☐ Certified copies of the priority documents have been received in Application No. _____.
  ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____.

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with requirements noted below. Failure to timely comply will result in ABANDONMENT of this application. THIS THREE-MONTH PERIOD IS NOT EXTENDABLE FOR SUBMITTING NEW FORMAL DRAWINGS, OR A SUBSTITUTE OATH OR DECLARATION. This three-month period for complying with the REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL is extendable under 37 CFR 1.136(a).

☐ Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL APPLICATION, PTO-152, which discloses that the oath or declaration is deficient. A SUBSTITUTE OATH OR DECLARATION IS REQUIRED.

☐ Applicant MUST submit NEW FORMAL DRAWINGS
  ☐ because the originally filed drawings were declared by applicant to be informal.
  ☐ including changes required by the Notice of Draftperson's Patent Drawing Review, PTO-948, attached hereto or to Paper No. _____.
  ☐ including changes required by the proposed drawing correction filed on _____, which has been approved by the examiner.
  ☐ including changes required by the attached Examiner's Amendment/Comment or in the Office action of Paper No. _____.

  Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings.

  ☐ Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Any reply to this notice should include, in the upper right hand corner, the APPLICATION NUMBER (SERIES CODE/SERIAL NUMBER). If applicant has received a Notice of Allowance and Issue Fee Due, the ISSUE BATCH NUMBER and DATE of the NOTICE OF ALLOWANCE should also be included.

Attachment(s)
  ☐ Notice of References Cited, PTO-892
  ☑ Information Disclosure Statement(s), PTO-1449, Paper No(s). _29_
  ☐ Notice of Draftsperson's Patent Drawing Review, PTO-948
  ☐ Notice of Informal Patent Application, PTO-152
  ☐ Interview Summary, PTO-413
  ☑ Examiner's Amendment/Comment
  ☐ Examiner's Comment Regarding Requirement for the Deposit of Biological Material
  ☐ Examiner's Statement of Reasons for Allowance

TAN T. NGUYEN
PRIMARY EXAMINER
GROUP 2800

PTOL-37 (Rev. 11/00)

1.   The Information Disclosure Statement submitted by Applicants on February 2,

2001 has been received and fully considered.

2.   The Formal Drawings submitted by Applicant on July 30, 2001 has been

received.

3:      Authorization for this examiner's amendment was given in a telephone interview

with Mr. Neil Steinberg on November 9, 2001.

4.   An examiner's amendment to the record appears below. Should the changes

and/or additions be unacceptable to applicant, an amendment may be filed as provided

by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be

submitted no later than the payment of the issue fee.

        In claim 151, line 6, before the words "wherein the first block size", the words --

wherein the memory device is capable of processing the first block size information,--

have been inserted.

        In claim 161, line 5, before the words "wherein the first block size ", the words --

wherein the memory device is capable of processing the first block size information,--

have been inserted.

        In claim 171, line 5, before the words "wherein the", the words --wherein the

memory device is capable of processing the first block size information--have been

inserted.

5.   Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Tan T. Nguyen whose telephone number is (703) 308-

1298. The examiner can normally be reached on Monday to Friday from 08:00 AM to 04:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Nelms, can be reached on (703) 308-4910. The fax phone number for the organization where this application or proceeding is assigned is (703) 308-7724.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Tan T. Nguyen
Primary Examiner
Art Unit 2818
November 09, 2001

#31(w #28

In the Application of:)   Group
)   Art Unit: 2818
    FARMWALD et al.   JUL 3 0 2001)
)   Before
Serial No: 09/492,982   )   Examiner: T. Nguyen
)
Filed: JANUARY 27, 2000   )
)
Title: METHOD OF OPERATING A MEMORY   )
        DEVICE HAVING A VARIABLE DATA   )
        INPUT LENGTH   )

Assistant Commissioner for Patents
Washington, DC 20231

Attn.: Official Draftsperson

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to the Commissioner of Patents and Trademarks, Washington, D.C. 20231 on *July 25 2001*
Michiko Sito
(Name of Person Mailing Correspondence)
Michiko Sito 7-25-01
Signature   Date

TRANSMITTAL OF FORMAL DRAWINGS

Dear Sir:

Enclosed herewith is one (1) set of fourteen (14) sheets of formal drawings for filing in the above-referenced patent application. The changes required by Applicants' proposed drawing corrections have been approved by the Examiner and incorporated into the attached formal drawings. In addition, the changes required as a result of the NOTICE OF DRAFTSPERSON'S PATENT DRAWING REVIEW (Hereinafter "NOTICE") dated July 13, 2001 have been incorporated. A copy of the NOTICE is enclosed herewith.

Applicants respectfully request that the enclosed drawings be accepted as formal drawings in the above-referenced application.

Respectfully submitted,

Date: _July 25, 2001_

Neil A. Steinberg
Reg. No. 34,735
650-947-5325

NOTICE OF DRAFTSPERSON'S
PATENT DRAWING REVIEW

492982

The drawing(s) filed (insert date) 12/08/00 are:

A. ☐ approved by the Draftsperson under 37 CFR 1.84 or 1.152.

B. ☒ objected to by the Draftsperson under 37 CFR 1.84 or 1.152 for the reasons indicated below. The Examiner will require submission of new, corrected drawings when necessary. Corrected drawings must be submitted according to the instructions on the back of this notice.

---

1. **DRAWINGS.** 37 CFR 1.84(a): Acceptable categories of drawings:
   Black ink. Color.
   ____ Color drawings are not acceptable until petition is granted.
   Fig(s) _____
   ____ Pencil and non black ink not permitted. Fig(s) _____

2. **PHOTOGRAPHS.** 37 CFR 1.84(b)
   ____ 1 full-tone set is required. Fig(s) _____
   ____ Photographs may not be mounted. 37 CFR 1.84(e)
   ____ Poor quality (half-tone). Fig(s) _____

3. **TYPE OF PAPER.** 37 CFR 1.84(e)
   ____ Paper not flexible, strong, white, and durable.
   Fig(s) _____
   ____ Erasures, alterations, overwritings, interlineations, folds, copy machine marks not accepted. Fig(s) _____
   ____ Mylar, velum paper is not acceptable (too thin).
   Fig(s) _____

4. **SIZE OF PAPER.** 37 CFR 1.84(f): Acceptable sizes:
   ____ 21.0 cm by 29.7 cm (DIN size A4)
   ____ 21.6 cm by 27.9 cm (8 1/2 x 11 inches)
   ____ All drawing sheets not the same size.
   Sheet(s) _____
   ____ Drawings sheets not an acceptable size. Fig(s) _____

5. **MARGINS.** 37 CFR 1.84(g): Acceptable margins:
   Top 2.5 cm Left 2.5cm Right 1.5 cm Bottom 1.0 cm
   SIZE: A4 Size
   Top 2.5 cm Left 2.5 cm Right 1.5 cm Bottom 1.0 cm
   SIZE: 8 1/2 x 11
   Margins not acceptable. Fig(s) _____
   ____ Top (T) ____ Left (L)
   ____ Right (R) ____ Bottom (B)

6. **VIEWS.** 37 CFR 1.84(h)
   REMINDER: Specification may require revision to correspond to drawing changes.
   Partial views. 37 CFR 1.84(h)(2)
   ____ Brackets needed to show figure as one entity.
   Fig(s) _____
   ____ Views not labeled separately or properly.
   Fig(s) _____
   ____ Enlarged views not labeled separately or properly.
   Fig(s) _____

7. **SECTIONAL VIEWS.** 37 CFR 1.84 (h)(3)
   ____ Hatching not indicated for sectional portions of an object.
   Fig(s) _____
   ____ Sectional designation should be noted with Arabic or Roman numbers. Fig(s) _____

8. **ARRANGEMENT OF VIEWS.** 37 CFR 1.84(i)
   ____ Words do not appear on a horizontal, left-to-right fashion when page is either upright or turned so that the top becomes the right side, except for graphs. Fig(s) _____

9. **SCALE.** 37 CFR 1.84(k)
   ____ Scale not large enough to show mechanism without crowding when drawing is reduced in size to two-thirds in reproduction.
   Fig(s) _____

10. **CHARACTER OF LINES, NUMBERS, & LETTERS.** 37 CFR 1.84(l)
    ____ Lines, numbers & letters not uniformly thick and well defined, clean, durable, and black (poor line quality).
    Fig(s) _____

11. **SHADING.** 37 CFR 1.84(m)
    ____ Solid black areas pale. Fig(s) _____
    ____ Solid black shading not permitted. Fig(s) _____
    ____ Shade lines, pale, rough and blurred. Fig(s) _____

12. **NUMBERS, LETTERS, & REFERENCE CHARACTERS.** 37 CFR 1.84(p)
    ____ Numbers and reference characters not plain and legible. Fig(s) _____
    ____ Figure legends are poor. Fig(s) _____
    ____ Numbers and reference characters not oriented in the same direction as the view. 37 CFR 1.84(p)(1) Fig(s) _____
    ____ English alphabet not used. 37 CFR 1.84(p)(2) Fig _____
    ____ Numbers, letters and reference characters must be at least .32 cm (1/8 inch) in height. 37 CFR 1.84(p)(3) Fig(s) _____

13. **LEAD LINES.** 37 CFR 1.84(q)
    ____ Lead lines cross each other. Fig(s) _____
    ____ Lead lines missing. Fig(s) _____

14. **NUMBERING OF SHEETS OF DRAWINGS.** 37 CFR 1.84(t)
    ____ Sheets not numbered consecutively, and in Arabic numerals beginning with number 1. Sheet(s) _____

15. **NUMBERING OF VIEWS.** 37 CFR 1.84(u)
    ____ Views not numbered consecutively, and in Arabic numerals, beginning with number 1. Fig(s) _____

16. **CORRECTIONS.** 37 CFR 1.84(w)
    ____ Corrections not made from prior PTO-948 dated _____

17. **DESIGN DRAWINGS.** 37 CFR 1.152
    ____ Surface shading shown not appropriate. Fig(s) _____
    ____ Solid black shading not used for color contrast. Fig(s) _____

COMMENTS

REVIEWER _____   DATE 7/13/01   TELEPHONE NO. 308-7001

ATTACHMENT TO PAPER NO. 25

6452863

FIG_1

RAM ARRAY 1

WORD LINES

ROW DECODE

5

BITLINES

6

3 COLUMN AMPLIFIERS

COLUMN SELECT

FIG_2

RESETOUT

RESETIN
BUSDATA[7]
•••
BUSDATA [1]
BUSDATA [0]
ADDRVALID
CLOCK1
CLOCK2
VREF
GND
V_{DD}

CPU — 11
DEVICE INTERFACE — 161

ROM — 12
DEVICE INTERFACE — 161

DRAM — 13
DEVICE INTERFACE — 161

DRAM — 14
DEVICE INTERFACE — 161

FIG_3

19
20
18
15
17 16

REGULAR ACCESS

ADDRVALID		CYCLE
1	BUSDATA[0:7]	0 – EVEN
	ACCESSTYPE[0:3] : MASTER[0:3]	
	ADDRESS[0:8]	1 – ODD
	ADDRESS[9:17]	2
	ADDRESS[18:26]	3
	ADDRESS[27:35]	4
0	ADDRESS[36:39] : BLOCKSIZE[0:3]	5

24
25
26
28
23
22
27

FIG_4

REJECT (NACK) CONTROL PACKET

	ADDRVALID	BUSDATA[0:7]	CYCLE
23	1	ACCESSTYPE[0:3] : MASTER[0:3] = 0	0 – EVEN
28	0	INFO[0:7]	1 – ODD

FIG_5

	ADDRVALID	BUSDATA[0:7]		CYCLE
23	1	ACCESSTYPE[0:3] : MASTER[0:3]	24	0
		ADDRESS[0:8]	25	1
22		ADDRESS[9:17]		2
		ADDRESS[18:26]		3
		ADDRESS[27:35]	26	4
27	1	ADDRESS[36:39] : BLOCKSIZE[0:3]	28	5
		XXX	29	6
	0	XXX	30	7
		XXX	31	8
	0	XXX	32	9
	0	INVALID: REQUEST[1:7]	33	10
29	0	REQUEST[8:15]	34	11

FIG_6

FIG_7A

VOLTAGE LOGICAL VALUE

2 — 0

V(a) AT 44   1.5 — 1

1 — >1

V(b) AT 45   0

1

46   47

T_F T_F

A ON B OFF   A OFF

TIME →

FIG. 7B

CLOCK1

CLOCK2

53

50

CLK

54

CHIP N

52

CHIP O

51

FIG_3A

55 56 57 58

CHIP N 52

55 56 57 58

CHIP O 51

59 60

FIG_3B

FIG. 3

CLK CLK̄

CLK

MULTIPLEXER

OUTPUT LINES

76

PAD 75

69

INPUT REC +/− 72

CLK 73

INPUT REC +/− 71

CLK̄ 74

INPUT REFERENCE 68

FIG. 10

FIG_11

SAMPLE

83

84

68

69

SENSE

INPUT −

INPUT +

INPUT REFERENCE

PAD

FIG_12

EARLY CLOCK 53

CLK1 — 100

LATE CLOCK 54

CLK2 — 110

DC AMP — 102

DELAY LINE — 103

116

CLOCKED RECEIVER — 101

CLOCKED RECEIVER — 111

FILTER

FILTER

DELAY = T_0 — 104

DELAY = $T_0 + X$ — 105

DELAY = $T_0 + X/2$ — 106

107

108

115

115

73

TO INPUT SAMPLERS

FIG. 13

Signal	Waveform labels
BUS CLOCK1 53	121 121
BUS CLOCK2 54	123 123
DELAY LINE OUTPUT 107	120 128 120
DELAY LINE OUTPUT 108	122 128 122
INTERNAL CLOCK 73	124 129 124 129
INTERNAL CLOCK COMPLEMENT 74	126 128 126
INPUT SAMPLE	125 127 125 127 128

CLOCK

RESET IN

RESET OUT

BUS DATA [0:7]　N　N + 1　N + 2

FIG. 14.

FIG_15

130

150

148	146 — 131
147 A 147 B	— 132
149	146 — 133
151	— 134
152	— 135
153	— 136
154	— 137
155	— 138
156	— 139
157	— 140

131
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PART B—ISSUE FEE TRANSMITTAL

Complete and mail this form, together with applicable fees, to:
Box ISSUE FEE
Assistant Commissioner for Patents
Washington, D.C. 20231

MAILING INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE. Blocks 1 through 4 should be completed where appropriate. All further correspondence including the Issue Fee Receipt, the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Legibly mark-up with any corrections or use Block 1)

1M41/0716

NEIL A STEINBERG ESQ
RAMBUS INC
4440 EL CAMINO REAL
LOS ALTOS CA 94022

Note: The certificate of mailing below can only be used for domestic mailings of the Issue Fee Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing.

Certificate of Mailing
I hereby certify that this Issue Fee Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Box Issue Fee address above on the date indicated below.

Michiko Sites   (Depositor's name)
Michiko Sites   (Signature)
July 25, 2001   (Date)

APPLICATION NO.	FILING DATE	TOTAL CLAIMS	EXAMINER AND GROUP ART UNIT	DATE MAILED
09/492,982	01/27/00	035	NGUYEN, T	2818	07/16/0

First Named Applicant: FARMWALD,   35 USC 154(b) term ext. = 0 Days;

TITLE OF INVENTION: METHOD OF OPERATING A MEMORY DEVICE HAVING A VARIABLE DATA INPUT LENGTH

ATTY'S DOCKET NO.	CLASS-SUBCLASS	BATCH NO.	APPLN. TYPE	SMALL ENTITY	FEE DUE	DATE DUE
3 P043D2C3C	365-233.000	J11	UTILITY	NO	$1240.00	10/16/0

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363). Use of PTO form(s) and Customer Number are recommended, but not required.

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" Indication (or "Fee Address" Indication form PTO/SB/47) attached.

2. For printing on the patent front page, list (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _Neil A. Steinberg_
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THIS PATENT (print or type)
PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. Inclusion of assignee data is only appropriate when an assignment has been previously submitted to the PTO or is being submitted under separate cover. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE
Rambus Inc.
(B) RESIDENCE (CITY & STATE OR COUNTRY)
Los Altos, California

Please check the appropriate assignee category indicated below (will not be printed on the patent)
☐ individual   ☒ corporation or other private group entity   ☐ government

4a. The following fees are enclosed (make check payable to Commissioner of Patents and Trademarks):
☐ Issue Fee
☐ Advance Order - # of Copies _____

4b. The following fees or deficiency in these fees should be charged to:
DEPOSIT ACCOUNT NUMBER _60-0998_
(ENCLOSE AN EXTRA COPY OF THIS FORM)
☒ Issue Fee
☒ Advance Order - # of Copies _5 copies_

The COMMISSIONER OF PATENTS AND TRADEMARKS is requested to apply the Issue Fee to the application identified above.

(Authorized Signature) _Neil Steinberg_   _Reg. No. 39,715_ (Date)
_7-25-01_

NOTE: The Issue Fee will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the Patent and Trademark Office.

08/02/2001 TEEDMBU2 00000061 500938 09492982
01 FC:142   1240.00 CH
02 FC:561   15.00 CH

Burden Hour Statement: This form is estimated to take 0.2 hours to complete. Time will vary depending on the needs of the individual case. Any comments on the amount of time required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, D.C. 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND FEES AND THIS FORM TO: Box Issue Fee, Assistant Commissioner for Patents, Washington D.C. 20231

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TRANSMIT THIS FORM WITH FEE

PTOL-85 (REV.10-96) Approved for use through 06/30/99. OMB 0651-0033   Patent and Trademark Office, U.S. DEPARTMENT OF COMMERCE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
(Case No. RA043D2C3C)

In the Application of:)
) Group Art Unit: 2818
        FARMWALD et al.   )
) Before Examiner: T. Nguyen
Serial No: 09/492,982   )
)
Filed: JANUARY 27, 2000   )
)
Title: METHOD OF OPERATING A   )
       MEMORY DEVICE HAVING A   )   FAX COPY RECEIVED
       VARIABLE DATA INPUT LENGTH   )
                                                        JAN 1 7 2002
Assistant Commissioner for Patents
Washington, DC 20231   TECHNOLOGY CENTER 2800

POWER OF ATTORNEY BY ASSIGNEE, REVOCATION OF ALL
PRIOR POWERS OF ATTORNEY AND CERTIFICATE UNDER 37 CFR 3.73(b)

Sir:

The undersigned, being empowered to sign this Power of
Attorney, Revocation of All Previous Powers of Attorney and
Certificate under 37 CFR 3.73(b) on behalf of Rambus Inc., the
assignee of the entire right, title and interest in the above-
referenced application, hereby revokes all prior powers of attorney
and hereby appoints Paul M. Anderson Reg. No. 39,896; Paula J.
Lagattuta, Reg No: 40,691 and Jose G. Moniz, P-50,192, jointly and
severally, with full power of substitution and revocation to
prosecute this application and to transact all business before the
United States Patent and Trademark Office in the above-referenced
application.

Rambus Inc. certifies that it is the assignee of the entire
right, title and interest in the above-referenced patent
application by virtue of an assignment from the inventors, Michael
Farmwald, and Mark Horowitz. The assignment of the prior parent

1

application.(Application serial No. 07/510,898) an all continuing and divisional applications thereof to Rambus Inc. was filed on April 18, 1990 and recorded in the U.S. Patent and Trademark Office at Reel 5385, Frame 875.

All the documents in the chain of title of the above-referenced application have been reviewed and, to the best of the undersigned's knowledge and belief, title is in Rambus Inc., the assignee identified above.
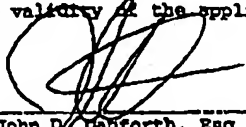
Please direct all correspondence in the above-referenced patent application to:

> Jose G. Moniz
> Rambus Inc.
> 4440 El Camino Real
> Los Altos, California 94022
> Telephone: 650-947-5336
> Facsimile: 650-947-5001

FAX COPY RECEIVED

JAN 1 7 2002

TECHNOLOGY CENTER 2800

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so as to make are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon.

Date: Jan 17, 2002

John D. Danforth, Esq.
Senior Vice President
General Counsel
Rambus Inc.

2

UNITED STATES PATENT AND TRADEMARK OFFICE

COMMISSIONER FOR PATENTS
UNITED STATES PATENT AND TRADEMARK OFFICE
WASHINGTON, D.C. 20231
www.uspto.gov

APPLICATION NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
09/492,982	01/27/2000	Michael Farmwald	P043D2C3C

CONFIRMATION NO. 1622

Jose G. Moniz
Rambus Inc.
4440 El Camino Real
Los Altos, CA 94022

OC000000008227102

Date Mailed: 06/04/2002

NOTICE REGARDING POWER OF ATTORNEY

This is in response to the Power of Attorney filed 01/17/2002.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

SARAH B MACKEY
2800 (703) 308-3066

OFFICE COPY
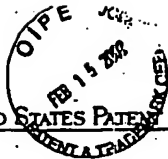
UNITED STATES PATENT AND TRADEMARK OFFICE

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UNITED STATES PATENT AND TRADEMARK OFFICE
WASHINGTON, D.C. 20231
www.uspto.gov

APPLICATION NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
09/492,982	01/27/2000	Michael Farmwald	P043D2C3C

CONFIRMATION NO. 1622

OC000000007070184

Neil A Steinberg Esq
Rambus Inc
4440 El Camino Real
Los Altos, CA 94022

Title: Method of operating a memory device having a variable data input length

Date Mailed: 11/14/2001

NOTICE OF PUBLICATION FEE DUE

The above-identified application was filed (including as a Continued Prosecution Application) on or after November 29, 2000 and a non-publication request in compliance with 37 CFR 1.213 was not included with the application on filing. Since the application has been allowed, a publication fee is due.

The fee due is $300.00. No small entity discount is available. See 37 CFR 1.18(d).

The reply to this notice should be mailed to:
Box ISSUE FEE
Commissioner for Patents
Washington D.C. 20231.

The publication fee must be submitted within THREE MONTHS from the mailing date of this notice or the application may be regarded as abandoned. No extensions of time under 37 CFR 1.136(a) or (b) are available. A reply must be filed to this notice, even if applicant does not anticipate that the application will be published (e.g., because the patent has issued and the projected publication date is more than a month after the issue date of the patent). A proper reply to this notice in such a situation would be a statement that no fee is now due, citing 37 CFR 1.211(e). If publication of the application does not occur, any publication fee paid will be refunded, if applicant requests a refund. See 37 CFR 1.211(e).

Questions relating to this Notice should be directed to the Office of Patent Publication at (703) 305-8283.

A copy of this notice should be returned with any reply.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In the Application of:)
)
    FARMWALD ET AL.)
)
Serial No.: 09/492,982) Patent No.: 6,452,863
)
Filed: January 27, 2000)
)
Title: METHOD OF OPERATING A MEMORY)
      DEVICE HAVING A VARIABLE DATA)
      INPUT LENGTH)

Certificate

NOV 2 6 2002

of Correction

Commissioner for Patents
Washington, DC 20231

REQUEST FOR CERTIFICATE OF CORRECTION UNDER 37 CFR §1.322

Dear Sir:

    It is respectfully requested that the Commissioner issue the attached Certificate of Correction to correct errors in U.S. Patent 6,452,863 B2 ("the '863 patent", copy attached). In particular, the attached Certificate of Correction seeks to correct errors in col. 26 of the '863 patent, namely, in claim 20 (line 7), claim 29 (line 43), and claim 34 (line 61).

    In the '863 patent, claim 20 (in col. 26, line 7) should include --14-- substituted for "11", since claim 20 should depend from claim 14 and not claim 11. The Preliminary Amendment of April 26, 2001, copy attached, clearly indicates claim 167 (renumbered as claim 20 in the '863 patent) being dependent from claim 161, which was renumbered as claim 14 in the '863 patent.

    In addition, an extraneous comma appears in the first line of claim 34 (col. 26). The Preliminary Amendment of April 26, 2001,

<div align="center">Page -1-</div>

NOV 2 6 2002

clearly shows that claim 177, renumbered as claim 34 in the '863 patent, includes no such comma.

Finally, the words "wherein the" are missing from the sixth line of claim 29 (col. 26). In the Supplemental Notice of Allowability mailed November 23, 2001, copy attached, an Examiner's amendment was authorized for claim 171, (renumbered as claim 29 in the '863 patent) which clearly indicates the words "wherein the" preceding the word "memory device", i.e., see page 2, item 4:

> In claim 171, line 5, before the words "wherein the", the words --wherein the memory device is capable of processing the first block size information—have been inserted. (emphasis added)

There were no subsequent amendments of the above-referenced application which affected the above-mentioned claims. Therefore, as is clearly disclosed by the records in the U.S. Patent and Trademark Office ("USPTO"), the errors mentioned herein incurred through the actions of the USPTO.

It is respectfully requested that the attached Certificate of Correction be issued. It is noted that should a telephone interview expedite consideration of this request in any way, kindly contact the undersigned at 650-947-5336.

Respectfully submitted,

Date: Nov 15, 2002

Jose G. Moniz
Agent of Record
Reg. No. 50,192
650-947-5336

Rambus Inc.
4440 El Camino Real
Los Altos, CA 94022

Page -2-

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO   : 6,452,863 B2

DATED   : Sept. 17, 2002

INVENTOR(S) : Farmwald et al.

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

col. 26, line 7, delete "11" and substitute --14--.

col. 26, line 43, insert --wherein the-- before "memory device".

col. 26, line 61, delete "," appearing between "delay" and "time".

MAILING ADDRESS OF SENDER:

Rambus Inc.
4440 El Camino Real
Los Altos, CA, 94022

PATENT NO. 6,452,863 B2

No. of additional copies

⇨

In the Application of:	)	
FARMWALD et al.	)	
	)	Group
Serial No: 09/492,982	)	Art Unit: 2818
	)	
Filed: JANUARY 27, 2000	)	Before
	)	Examiner: T. Nguyen
Title: METHOD OF OPERATING A MEMORY	)	
DEVICE HAVING A VARIABLE DATA	)	
INPUT LENGTH	)	

Assistant Commissioner for Patents
Washington, DC 20231

AMENDMENT

Dear Sir:

　　　Kindly amend the application as follows:

IN THE CLAIMS:

　　　Please **substitute** the following claims for the pending claims

having the same claim number:

　　　(A marked-up version showing insertions and deletions to the

pending claims is attached as EXHIBIT A)

1   151. (Amended) A method of controlling a memory device by a

2   memory controller, wherein the memory device includes a plurality of

3   memory cells, the method of controlling the memory device

4   comprises:

5   providing first block size information to the memory device,

6   wherein the first block size information is provided by the memory

7   controller and is representative of a first amount of data to be input

8   by the memory device; and

9   issuing a first operation code to the memory device, wherein in

10   response to the first operation code, the memory device inputs the

11   first amount of data.

1   152. The method of claim 151 wherein the memory device inputs the

2   first amount of data synchronously with respect to an external clock

3   signal.

1   153. (Amended) The method of claim 151 further including:

2   providing second block size information to the memory device,

3   wherein the second block size information defines a second amount of

4   data to be input by the memory device; and

5   issuing a second operation code to the memory device, wherein in

6   response to the second operation code, the memory device inputs the

7   second amount of data.

1   154. (Amended) The method of claim 151 wherein the first block

2   size information and the first operation code are included in a request

3   packet.

1   155. (Amended) The method of claim 154 wherein the first block

2   size information and the first operation code are included in the same

3   request packet.

1   156. (Amended) The method of claim 151 further including providing
2   the first amount of data to the memory device.

1   157. (Amended) The method of claim 156 wherein the first amount
2   of data is provided to the memory device after a delay time transpires.

1   158. (Amended) The method of claim 157 wherein the delay time is
2   representative of a number of clock cycles of an external clock signal.

1   159. (Amended) The method of claim 151 wherein the first block
2   size information is a binary representation of the first amount of
3   data.

1   160. (Amended) The method of claim 151 wherein the first amount
2   of data is output, by the memory controller, synchronously with respect
3   to an external clock signal and during a plurality of clock cycles of
4   the external clock signal.

1   161. (Amended) A method of operation in a synchronous memory
2   device, wherein the memory device includes a plurality of memory cells,
3   the method of operation of the memory device comprises:
4   receiving first block size information from a memory controller,
5   wherein the first block size information represents a first amount of
6   data to be input by the memory device in response to an operation code;
7   receiving the operation code, from the memory controller,
8   synchronously with respect to an external clock signal; and
9   inputting the first amount of data in response to the operation
10   code.

1   162. (Amended) The method of claim 161 wherein inputting the first
2   amount of data includes receiving the first amount of data
3   synchronously with respect to the external clock signal.

Page 3

1   163. (Amended) The method of claim 162 wherein the first amount
2   of data is sampled over a plurality of clock cycles of the external
3   clock signal.

1   164. (Amended) The method of claim 161 wherein the first block
2   size information and the operation code are included in a request
3   packet.

1   165. (Amended) The method of claim 164 wherein the first block
2   size information and the operation code are included in the same
3   request packet.

1   166. (Amended) The method of claim 161 wherein the first block
2   size information is a binary representation of the first amount of data
3   to be input in response to the operation code.

1   167. (Amended) The method of claim 161 wherein the first amount
2   of data is output, by the memory controller, synchronously during a
3   plurality of clock cycles of the external clock signal.

1   168. (Amended) The method of claim 161 further including
2   generating an internal clock signal, using a delay locked loop and the
3   external clock signal wherein the first amount of data is input
4   synchronously with respect to the internal clock signal.

1   169. (Amended) The method of claim 161 further including
2   generating first and second internal clock signals using clock
3   generation circuitry and the external clock signal, wherein the first
4   amount of data is input synchronously with respect to the first and
5   second internal clock signals.

1   170. The method of claim 169 wherein the first and second internal
2 clock signals are generated by a delay lock loop.

1   171. (Amended) A method of operation of an integrated circuit,
2 wherein the integrated circuit includes a dynamic random access memory
3 array having a plurality of memory cells, the method of operation
4 comprises:
5   receiving block size information from a controller, wherein the
6 block size information represents an amount of data to be input in
7 response to an operation code;
8   receiving the operation code from the controller; and
9   inputting the amount of data in response to the operation
10 code.

1   172. (Amended) The method of claim 171 further including storing
2 the amount of data in the memory array.

1   173. (Amended) The method of claim 171 wherein the block size
2 information and the operation code are included in a request
3 packet.

1   174. (Amended) The method of claim 171 wherein the block size
2 information is a binary representation of the amount of data to be
3 input in response to the operation code.

1   176. (Amended) The method of claim 171 wherein the amount of data
2 is input, in response to the operation code, after a delay time
3 transpires.

1   177. The method of claim 176 wherein the delay time is
2 representative of a number of clock cycles of the external clock
3 signal.

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Kindly ADD the following claims:

1   178. (New) The method of claim 151 wherein the first operation
2   code is issued onto a bus.

1   179. (New) The method of claim 178 wherein the bus includes a
2   plurality of signal lines to multiplex control information, address
3   information and data.

1   180. (New) The method of claim 151 further including providing
2   address information to the memory device.

1   181. (New) The method of claim 161 wherein the operation code, the
2   first block size information and address information are included in a
3   packet.

1   182. (New) The method of claim 161 further including receiving
2   address information from the memory controller.

1   183. (New) The method of claim 161 wherein the first block size
2   information, and the operation code are received from an external bus.

1   184. (New) The method of claim 183 wherein the first block size
2   information, and the operation code are received from the same external
3   bus.

1   185. (New) The method of claim 184 wherein the external bus is
2   used to multiplex address information, control information and
3   data.

1   186. (New) The method of claim 171 further including receiving
2   address information from the controller.

<u>REMARKS</u>

This Preliminary Amendment seeks to place this application in condition for allowance. New claims 178-186 have been added to more fully claim Applicant's invention. Several of the pending claims have been amended. No new matter has been added. In this regard, support may be found, for example, at page 22, line 11, to page 24, line 2, and page 27, lines 1-24 of the specification.

INFORMATION DISCLOSURE STATEMENT

In compliance with the duty of disclosure set forth in 37 C.F.R. §1.56, Applicants' submit concurrently herewith an Information Disclosure Statement (IDS) including modified Form PTO-1449. A <u>copy</u> of that IDS and modified Form PTO-1449 are attached hereto.

Some of the documents listed in the PTO-1449 have been cited by a defendant in an action pending in U.S. District Court For Eastern District of Virginia case, namely in <u>Rambus Inc. v. Infineon Technologies A.G., et al.</u>, as prior art against the inventions claimed in, among other patents, U.S. 6,034,918. The '918 patent is a parent of the instant application. Reference to these documents are listed on page 2 of the Defendents' AMENDED PRIOR ART NOTICE PURSUANT TO 35 U.S.C. §282 (hereinafter 'PRIOR ART NOTICE'). A copy of the PRIOR ART NOTICE is included with the IDS submission.

Furthermore, the construction or interpretation of a number of terms have recently been considered in a *Markman* opinion issued in the above-mentioned litigation. A number of claims pending in the instant application incorporate or incorporated some of these terms including, for example, the terms "block size", "write request", and "bus". The term "write request" has been deleted from the pending claims (as amended). The term "bus" has been deleted from some of the pending claims (as amended). A discussion of "block size" may be found on pages 41-47 of the *Markman* opinion, and a discussion of "bus" may be

Page 7

found on pages 17-41 of the *Markman* opinion. By submission of this *Markman* opinion, Applicants make no statement as to the correctness of the constructions set forth therein. Indeed, as is apparent from that opinion, the court substantially adopted the constructions proposed by Infineon, and not that construction proposed by Rambus. A copy of the *Markman* opinion is also included with the IDS submission.

CONCLUSION

Applicants request entry of the foregoing amendment. Applicants submit that all of the claims present patentable subject matter which definitely set forth the novel and unobvious features of Applicants' invention. Accordingly, Applicants respectfully request allowance of all of the claims.

It is noted that should a telephone interview expedite the prosecution in any way, the Examiner is invited to contact Neil Steinberg at 650-947-5325.

Respectfully submitted,

Date: April 26, 2001

Neil A. Steinberg
Reg. No. 34,735
650-947-5325

Page 8

1   151. (Amended) A method of controlling a memory device by a memory

2   controller, wherein the memory device includes a plurality of memory

3   cells, the method of controlling the memory device comprises:

4   providing first block size information to the memory device,

5   wherein the first block size information is provided by the memory

6   controller and [defines] is representative of a first amount of data to

7   be input by the memory device [in response to a write request]; and

8   issuing a first operation code [write request] to the memory

9   device, wherein in response to the first operation code, [write

10   request] the memory device inputs the first amount of data

11   [corresponding to the first block size information].

1   152. The method of claim 151 wherein the memory device inputs the

2   first amount of data synchronously with respect to an external clock

3   signal.

1   153. (Amended) The method of claim 151 further including:

2   providing second block size information to the memory device,

3   wherein the second block size information defines a second amount of

4   data to be input by the memory device [in response to a write request];

5   and

6   issuing a second operation code [write request] to the memory

7   device, wherein in response to the second operation code [write

8   request], the memory device inputs the second amount of data

9   [corresponding to the second block size information].

1   154. (Amended) The method of claim 151 wherein the first block

2   size information and the first operation code [write request] are

3   included in a request packet.

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1   155. (Amended) The method of claim 154 wherein the first block

2   size information and the first operation code [write request] are

3   included in the same request packet.

1   156. (Amended) The method of claim 151 further including providing

2   the first amount of data [corresponding to the first block size

3   information] to the memory device.

1   157. The method of claim 156 wherein the first amount of data is

2   provided to the memory device after a delay time transpires.

1   158. (Amended) The method of claim 157 [156] wherein the delay

2   time is representative of a number of clock cycles of [a] an external

3   clock signal.

1   159. (Amended) The method of claim 151 wherein the first block

2   size information is a binary representation of the first amount of data

3   [to be input in response to the first write request].

1   160. (Amended) The method of claim 151 wherein the first amount

2   of data [corresponding to the first block size information] is output,

3   by the memory controller, [input] synchronously during a plurality of

4   clock cycles of an [the] external clock signal.

1   161. (Amended) A method of operation in a synchronous memory

2   device, wherein the memory device includes a plurality of memory cells,

3   the method of operation of the memory device comprises:

4   receiving first block size information from a memory controller,

5   wherein the first block size information [defines] represents a first

6   amount of data to be input by the memory device in response to the

7   operation code [a write request];

Page 10

8   receiving an operation code, [a first write request] from the

9   memory controller, synchronously with respect to an external clock

10   signal; and

11   inputting the first amount of data [corresponding to the first

12   block size information] in response to the operation code [first write

13   request].

1   162. (Amended) The method of claim 161 wherein inputting the first

2   amount of data includes receiving the first amount of data [the first

3   amount of data corresponding to the first block size information is

4   sampled] synchronously with respect to the external clock signal.

1   163. (Amended) The method of claim 161 wherein the first amount

2   of data is sampled synchronously during a plurality of clock cycles of

3   the external clock signal [further including:

4   [receiving second block size information, wherein the second block

5   size information defines a second amount of data to be input in

6   response to a write request;

7   receiving a second write request from the bus controller; and

8   inputting the second amount of data corresponding to the second

9   block size information], in response to the second operation code write

10 request].

1   164. (Amended) The method of claim 161 wherein the first block

2   size information and the operation code [first write request] are

3   included in a request packet.

1   165. (Amended) The method of claim 164 wherein the first block

2   size information and the operation code [first write request] are

3   included in the same request packet.

Page 11

1 166. (Amended) The method of claim 161 wherein the first block

2 size information is a binary representation of the first amount of data

3 to be input in response to the <u>operation code</u> [first write

4 request].

1 167. (Amended) The method of claim 161 wherein the first amount

2 of data [corresponding to the first block size information] is [input]

3 <u>output, by the memory controller,</u> synchronously during a plurality of

4 clock cycles of [an] <u>the</u> external clock signal.

1 168. (Amended) The method of claim 161 further including

2 generating an internal clock signal using a delay locked loop and <u>the</u>

3 [an] external clock signal, wherein the first amount of data

4 [corresponding to the first block size information] is input

5 synchronously with respect to the internal clock signal.

1 169. (Amended) The method of claim 161 further including

2 generating first and second internal clock signals using clock

3 generation circuitry and [an] <u>the</u> external clock signal, wherein the

4 first amount of data [corresponding to the first block size

5 information] is input synchronously with respect to the first and

6 second internal clock signals.

1 170. The method of claim 169 wherein the first and second internal

2 clock signals are generated by a delay lock loop.

1 171. (Amended) A method of operation of an integrated circuit,

2 wherein the integrated circuit includes a <u>dynamic random access</u> memory

3 array having a plurality of memory cells, the method of operation

4 comprises:

5 receiving block size information from a controller, wherein the

6 block size information [defines a first] <u>represents an</u> amount of data

Page 12

7   to be input [from a bus] in response to <u>an operation code</u> [a write

8   request];

9   receiving <u>the operation code from the controller</u> [a first write

10   request]; and

11   inputting the [first] amount of data [corresponding to the block

12   size information] in response to the <u>operation code</u> [first write

13   request].

1   172. (Amended) The method of claim 171 further including storing

2   the [first] amount of data [corresponding to the block size

3   information] in the memory array.

1   173. (Amended) The method of claim 171 wherein the block size

2   information and the <u>operation code</u> [first write request] are included

3   in a request packet.

1   174. (Amended) The method of claim 171 wherein the block size

2   information is a binary representation of the [first] amount of data to

3   be input in response to the <u>operation code</u> [first write request].

1   176. (Amended) The method of claim 171 [161] wherein the [first]

2   amount of data is input, in response to [receipt of] the <u>operation code</u>

3   [first write request], after a delay time transpires.

1   177. The method of claim 176 wherein the delay time is

2   representative of a number of clock cycles of the external clock signal

3   [that transpire before the first amount of data is input].

1   178. (New) The method of claim 151 wherein the first operation

2   code is issued onto a bus.

Page 13

1   179. (New) The method of claim 178 wherein the bus includes a
2   plurality of signal lines to multiplex control information, address
3   information and data.

1   180. (New) The method of claim 151 further including providing
2   address information to the memory device.

1   181. (New) The method of claim 161 wherein the operation code, the
2   first block size information and address information are included in a
3   packet.

1   182. (New) The method of claim 161 further including receiving
2   address information from the memory controller.

1   183. (New) The method of claim 161 wherein the first block size
2   information, and the operation code are received from an external bus.

1   184. (New) The method of claim 183 wherein the first block size
2   information, and the operation code are received from the same external
3   bus.

1   185. (New) The method of claim 184 wherein the external bus is
2   used to multiplex address information, control information and
3   data.

1   186. (New) The method of claim 171 further including receiving
2   address information from the controller.

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/492,982	01/27/2000	Michael Farmwald	P043D2C3C	1622

7590

Neil A Steinberg Esq
Rambus Inc
4440 El Camino Real
Los Altos, CA 94022

NOV 2 2 2002

EXAMINER
NGUYEN, TAN

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 11/23/2001

Please find below and/or attached an Office communication concerning this application or proceeding.

FO-90C (Rev. 07-01)

NOV 2 2 2002

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.

EXAMINER

ART UNIT	PAPER NUMBER
	30

DATE MAILED:

This is a communication from the examiner in charge of this application.
COMMISSIONER OF PATENTS AND TRADEMARKS *SUPPLEMENTAL*

NOTICE OF ALLOWABILITY

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance and Issue Fee Due or other appropriate communication will be mailed in due course. THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS. This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

☑ This communication is responsive to *the IDS filed on 02/02/01*

☑ The allowed claim(s) is/are *151 - 186*

☑ The drawings filed on *02/02/01* are acceptable as formal drawings.

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

☐ All ☐ Some* ☐ None of the:
    ☐ Certified copies of the priority documents have been received.
    ☐ Certified copies of the priority documents have been received in Application No. _____
    ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with requirements noted below. Failure to timely comply will result in ABANDONMENT of this application. THIS THREE-MONTH PERIOD IS NOT EXTENDABLE FOR SUBMITTING NEW FORMAL DRAWINGS, OR A SUBSTITUTE OATH OR DECLARATION. This three-month period for complying with the REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL is extendable under 37 CFR 1.136(a).

☐ Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL APPLICATION, PTO-152, which discloses that the oath or declaration is deficient. A SUBSTITUTE OATH OR DECLARATION IS REQUIRED.

☐ Applicant MUST submit NEW FORMAL DRAWINGS
    ☐ because the originally filed drawings were declared by applicant to be informal.
    ☐ including changes required by the Notice of Draftperson's Patent Drawing Review, PTO-948, attached hereto or to Paper No.____
    ☐ including changes required by the proposed drawing correction filed on _____, which has been approved by the examiner.
    ☐ including changes required by the attached Examiner's Amendment/Comment or in the Office action of Paper No.____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings.

☐ Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Any reply to this notice should include, in the upper right hand corner, the APPLICATION NUMBER (SERIES CODE/SERIAL NUMBER). If applicant has received a Notice of Allowance and Issue Fee Due, the ISSUE BATCH NUMBER and DATE of the NOTICE OF ALLOWANCE should also be included.

Attachment(s)
☐ Notice of References Cited, PTO-892
☑ Information Disclosure Statement(s), PTO-1449, Paper No(s). *29*
☐ Notice of Draftperson's Patent Drawing Review, PTO-948
☐ Notice of Informal Patent Application, PTO-152
☐ Interview Summary, PTO-413
☑ Examiner's Amendment/Comment
☐ Examiner's Comment Regarding Requirement for the Deposit of Biological Material
☐ Examiner's Statement of Reasons for Allowance

TAN T. NGUYEN
PRIMARY EXAMINER
GROUP 2800

PTOL-37 (Rev. 11/00)

1.   The Information Disclosure Statement submitted by Applicants on February 2,

2001 has been received and fully considered.

2.   The Formal Drawings submitted by Applicant on July 30, 2001 has been

received.

3.   Authorization for this examiner's amendment was given in a telephone interview

with Mr. Neil Steinberg on November 9, 2001.

4.   An examiner's amendment to the record appears below. Should the changes

and/or additions be unacceptable to applicant, an amendment may be filed as provided

by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be

submitted no later than the payment of the issue fee.

In claim 151, line 6, before the words "wherein the first block size", the words --

wherein the memory device is capable of processing the first block size information,--

have been inserted.

In claim 161, line 5, before the words "wherein the first block size ", the words --

wherein the memory device is capable of processing the first block size information,--

have been inserted.

In claim 171, line 5, before the words "wherein the", the words --wherein the

memory device is capable of processing the first block size information--have been

inserted.

5.   Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Tan T. Nguyen whose telephone number is (703) 308-

1298. The examiner can normally be reached on Monday to Friday from 08:00 AM to 04:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Nelms, can be reached on (703) 308-4910. The fax phone number for the organization where this application or proceeding is assigned is (703) 308-7724.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Tan T. Nguyen
Primary Examiner
Art Unit 2818
November 09, 2001

PTO-1449 (Modified)	ATTY. DOCKET NO. P043D2C3C	SERIAL NUMBER 09/492,982
U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	APPLICANT(S) FARMWALD ET AL	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	FILING DATE JANUARY 27, 2000	GROUP ART UNIT 2818

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
TNT	4,763,249	08/09/88	Bomba et al	364	200	
/	4,394,753	07/19/83	Penzel	365	236	
/	4,785,428	11/15/88	Bajwa	365	233	
TNT	4,680,738	07/14/87	Tam	365	239	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER Tan T. Nguyen	DATE CONSIDERED 11/08/01

EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant.

NOTICE RE: CERTIFICATES OF CORRECTION

DATE : 12/30/2002   Paper No.: 36

TO : Supervisor, Art Unit 2800

SUBJECT : Certificate of Correction Request in Patent No.: 6452863

A response to the following question is requested with respect to the accompanying request for a certific of correction.

With respect to the change(s) requested, correcting Office and/or Applicant's errors, should the patent read as shown in the certificate of correction? No new matter should be introduced, nor should tl scope or meaning of the claims be changed.

*PLEASE COMPLETE THIS FORM AND
RETURN WITH FILE, WITHIN 7 DAYS,
TO CERTIFICATES OF CORRECTION BRANCH - PK 3-915/922
PALM LOCATION 7580 - TEL. NO. 305-8309*

THANK YOU FOR YOUR ASSISTANCE!

Note your decision, regarding the changes requested in the Request for Certificate of Correction, placing a check mark (+) in the box that reflects your decision, which corresponds to the question check above.

☒ YES   ☐ NO   ☐ Comments below

☐ Comments:

_____

_____

_____

_____

_____

_____   2818
Supervisor   Art Unit

863 FH PG 0555

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,452,863 B2   Page 1 of 1
DATED : September 17, 2002
INVENTOR(S) : Farmwald et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:
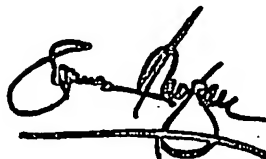
<u>Column 26,</u>
Line 7, delete "11" and substitute -- 14 --.
Line 43, insert -- wherein the -- before "memory device".
Line 61, delete "," appearing between "delay" and "time".

Signed and Sealed this

First Day of April, 2003

JAMES E. ROGAN
Director of the United States Patent and Trademark Office

/1/

PATENT APPLICATION FEE DETERMINATION RECORD
Effective December 29, 1999

Application or Docket Number

CLAIMS AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY TYPE ☐ RATE	FEE	OR	OTHER THAN SMALL ENTITY RATE	FEE
BASIC FEE				345.00	OR		690.00
TOTAL CLAIMS	25 minus 20=	5	X$ 9=		OR	X$18=	
INDEPENDENT CLAIMS	2 minus 3 =		X39=		OR	X78=	
MULTIPLE DEPENDENT CLAIM PRESENT			+130=		OR	+260=	
					OR	TOTAL	1900

* If the difference in column 1 is less than zero, enter "0" in column 2

CLAIMS AS AMENDED - PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT	(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE	ADDITIONAL FEE	OR	OTHER THAN SMALL ENTITY RATE	ADDITIONAL FEE
Total	•	Minus **	=	X$ 9=		OR	X$18=	
Independent	-	Minus ***	=	X39=		OR	X78=	
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				+130=		OR	+260=	
				TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT	(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE	ADDITIONAL FEE	OR	RATE	ADDITIONAL FEE
Total	27	Minus ** 25	= 2	X$ 9=		OR	X$18=	36
Independent	3	Minus *** 3	= —	X39=		OR	X78=	
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				+130=		OR	+260=	
				TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	36

AMENDMENT C

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT	(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE	ADDITIONAL FEE	OR	RATE	ADDITIONAL FEE
Total	27	Minus ** 27	=	X$ 9=		OR	X$18=	
Independent	3	Minus *** 3	=	X39=		OR	X78=	
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				+130=		OR	+260=	
				TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

FORM PTO-875
(Rev. 12/99)

Patent and Trademark Office, U.S. DEPARTMENT OF COMMERCE

PATENT APPLICATION FEE DETERMINATION RECORD Effective December 29, 1999	Application or Docket Number 09/492482

CLAIMS AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA
BASIC FEE		
TOTAL CLAIMS	26 minus 20=	6
INDEPENDENT CLAIMS	3 minus 3 =	0
MULTIPLE DEPENDENT CLAIM PRESENT		

SMALL ENTITY TYPE ☐			OTHER THAN SMALL ENTITY	
RATE	FEE	OR	RATE	FEE
	345.00	OR		
X$ 9=		OR	X$18=	
X40=		OR	X80=	
+130=		OR	+260=	
TOTAL		OR	TOTAL	

* If the difference in column 1 is less than zero, enter "0" in column 2

CLAIMS AS AMENDED - PART II

AMENDMENT A		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
	Total	•	Minus	••	=
	Independent	•	Minus	•••	=
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				

SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
RATE	ADDI-TIONAL FEE		RATE	ADDI-TIONAL FEE
X$ 9=		OR	X$18=	
X40=		OR	X80=	
+130=		OR	+260=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT B		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
	Total	•	Minus	••	=
	Independent	•	Minus	•••	=
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				

RATE	ADDI-TIONAL FEE		RATE	ADDI-TIONAL FEE
X$ 9=		OR	X$18=	
X40=		OR	X80=	
+130=		OR	+260=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT C		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
	Total	•	Minus	••	=
	Independent	•	Minus	•••	=
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				

RATE	ADDI-TIONAL FEE		RATE	ADDI-TIONAL FEE
X$ 9=		OR	X$18=	
X40=		OR	X80=	
+130=		OR	+260=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

nique for linear integrated circuits," *IEEE J. Solid-State Circuits*, vol. SC-4, pp. 110–122, June 1969.

[16] F. W. Hewlett, Jr., "I²L current gain design," *IEEE J. Solid-State Circuits*, vol. SC-12, pp. 206–208, Apr. 1977.

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A Programmable NMOS DRAM Controller for Microcomputer Systems with Dual-Port Memory and Error Checking and Correction

MEL BAZES, JAMES NADIR, DAVID PERLMUTTER, BENI MANTEL, AND OMER ZAK

Abstract—An NMOS DRAM controller for use in microcomputer systems based on the iAPX-86 and iAPX-286 microprocessor families or on the Multibus system bus is described. The controller provides complete support for dual-port memories and memories with error checking and correction. The controller has programmable attributes for configuring it to the particular requirements of the system. The controller uses parallel arbitration to minimize arbitration delay. A memory cycle will start on the same clock edge that samples a command if the cycle has been previously enabled. Novel logic and circuit design techniques have been used to achieve 16 MHz operation, 20 ns input setup time, and 35 ns output delay time.

I. INTRODUCTION

THE advantages of using dynamic RAM (DRAM) over static RAM (SRAM) outweigh the disadvantages in many memory applications. The savings provided by DRAM in cost, board space, and power usually more than offset its cumbersome control and refresh requirements. The lower performance of DRAM in comparison to SRAM, as measured by access time, is still more than adequate for a large number of system applications.

To benefit from the full potential of DRAM, a memory designer often has to design a relatively complex controller for interfacing the DRAM to the rest of the system. The most basic function of this controller is twofold: to translate system
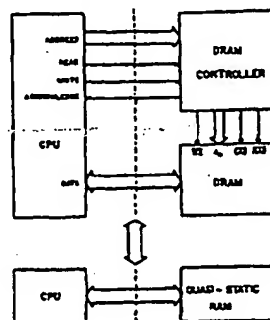
Fig. 1. Conversion of Dynamic RAM to quad-static RAM by a Dynamic RAM controller.
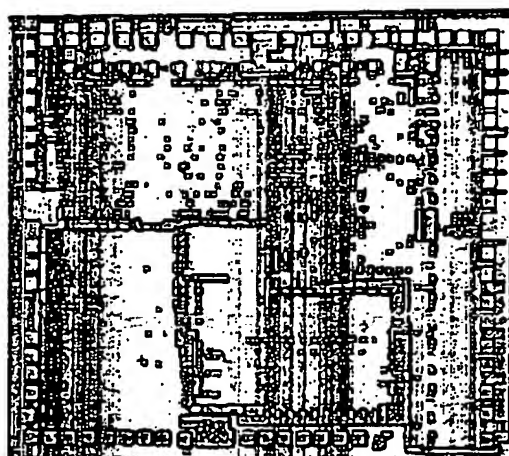
Fig. 2. ADC photomicrograph.

commands, such as ordinary READ's and WRITE's, into the sequence of signals "understood" by DRAM; and to perform maintenance functions, in the form of "wake-up" cycles, after power-up and periodic refresh cycles thereafter.

In the most general sense, the function of a DRAM controller is to give the appearance to the system that the memory is static. Fig. 1 illustrates this concept.

The DRAM control function, in spite of its essential character and widespread applicability (every DRAM-based memory needs one), paradoxically does not lend itself very well to implementation as a general-purpose LSI function. This situation stems from the multitude of system configurations and performance requirements a controller would have to be able to support in order to earn the designation "general purpose." A truly general purpose, high-performance integrated controller would probably be too costly to be attractive to a memory designer—if the memory designer could not use more than a

small subset of all the features provided by the controller, he would be loathe to pay for all of them. A more practical approach to integrating the control function is to partition the range of control applications into subranges and to define general purpose high-performance integrated solutions for individual subranges.

This paper describes a general purpose, high-performance integrated controller for one of the subranges of controller applications: the Advanced Dynamic RAM Controller (ADC)[1] is a programmable DRAM controller for memories directly interfacing to the iAPX-86 [1] and iAPX-286 [2] classes of microprocessor and to the Multibus system bus [3]. It is implemented in HMOSII [4], an NMOS technology. A photomicrograph of the chip appears in Fig. 2. The paper first describes some important controller functions provided by the

[1] Intel 8207.

chip, then discusses the internal organization of the chip, and finally lists several design attributes of the chip and presents some novel logic and circuit design techniques used in achieving performance goals.

II. CONTROLLER FUNCTIONS

Beyond the basic DRAM-control function of performing READ's, WRITE's, and refreshes, the ADC also provides control options in support of specialized memory applications. The options discussed below are dual-port memory, error checking and correction, and programmable controller attributes.

A. Dual-Port Memory

Two independent microprocessor/bus interfaces, or ports, are provided. Each port may be independently programmed to be configured to the microprocessor/bus type connected to the port. The programmable port attributes are

1) Microprocessor or bus type.
2) Synchronous or asynchronous commands.
3) Acknowledge type.

Attribute 1 is a function of the timing and format of command signals from the particular microprocessor/bus connected to the port. Attribute 2 determines whether or not internal synchronizer flip-flops will be inserted in the path of the commands in order to synchronize the commands with the chip clock. Attribute 3 determines whether the port returns an advanced acknowledge, i.e., an acknowledge arriving a fixed time *before the end* of the cycle, or whether it returns a transfer acknowledge, i.e., an acknowledge arriving *at the end* of the cycle.

Fig. 3 illustrates schematically a dual-port memory using the ADC. The ADC arbitrates between the two ports in such a way that commands are serviced as quickly as possible, with neither port monopolizing memory, i.e., "shutting out" the other port through the sheer rate at which it outputs commands.

The priority granted to each port, and to the third contender for service, refresh, is dynamically modified on the basis of a set of arbitration rules and on the basis of the recent history of service granted to each port.

A LOCK control is provided for those instances, such as test-and-set operations, semaphore operations, or high-speed block transfers, in which one port must not relinquish its access to memory in favor of the other port. When one port activates LOCK, the other port is denied service until LOCK is deactivated. Refresh is not affected by LOCK.

B. Error Checking and Correction

When used with its companion chip, the error detection and correction unit (EDCU)[2] [5], the ADC provides complete error checking and correction (ECC) [6] service for memory. Fig. 4 illustrates schematically a memory with ECC controlled by the ADC.

In ECC, every data word has a unique set of check bits

[2] Intel 8206
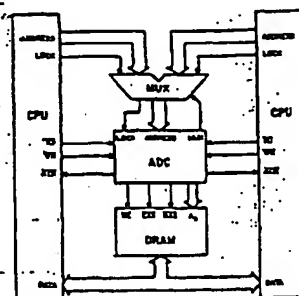
Fig. 3. Dual-port memory controlled by ADC.
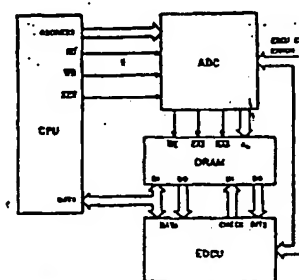
Fig. 4. Memory with ECC controlled by ADC and EDCU.

stored along with the word in memory. The check bits are generated by the EDCU using a modified Hamming code. Whenever a data word is read out of memory it is checked for errors using the check bits read out with the word. An error in only one bit is correctable, while an error in two or more bits is uncorrectable. The error description—given by the error type (correctable or uncorrectable), bit in error (for single-bit errors only), and word address—may be latched for error-logging purposes. The system may use the error description in order to take appropriate action in the case of memory errors, e.g., by remapping memory to delete a faulty memory card.

Multiple-bit errors generally result from the accumulation of single-bit errors in a particular memory location over a long period of time. To minimize the occurrence of multiple-bit errors, the ADC automatically performs periodic *memory scrubbing* on all memory locations once every 16.4 s. A memory location is scrubbed by simply performing a READ operation on the location and correcting a single-bit error if one is present. Memory scrubbing is performed simultaneously during refresh cycles, with one memory location scrubbed per refresh. Thus, no memory location, even one seldom accessed by the system, is allowed to go too long without ECC. Since memory scrubbing occurs only during refresh cycles, no performance penalty is paid for it.

At power-up, memory contents are indefinite and would
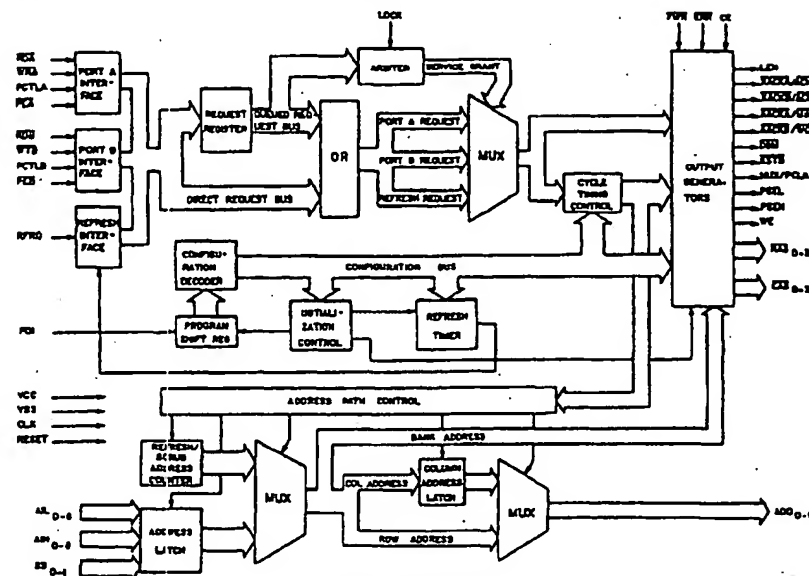
Fig. 5. ADC block diagram.

produce uncorrectable errors in READ-MODIFY-WRITE operations. In order to prevent false errors from being flagged, the ADC automatically initializes all of memory after power-up to zero with the proper check bits.

C. Programmable Control Attributes

Several attributes of the ADC are modifiable through programming to match it to the memory being controlled. Some of the modifiable attributes are outlined below.

1) DRAM Speed—Memory cycles matched to either of two common DRAM speeds may be selected: $t_{RAC} = 100$ ns or $t_{RAC} = 150$ ns.

2) Word Length—Memory may be configured with word lengths of from 8 bits up to 80 bits, not counting check bits.

3) Refresh Mode—Refreshes may be initiated internally or externally. Internally initiated refreshes are always single refresh cycles, while externally initiated refreshes may be single cycles or 128-cycle bursts. A refresh cycle may be programmed to be initiated internally if an external refresh request is late in arriving.

4) Refresh Rate—The internal refresh timer can be programmed to provide 256 refreshes every 4 ms or every 2 ms for up to 16 different operating frequencies.

III. INTERNAL ORGANIZATION

A block diagram of the ADC appears in Fig. 5. In the most general sense, the chip is organized into three sections:

1) Initialization and configuration.
2) Service request and output signal generation.
3) Address path.

A description of each section is given below.

A. Initialization and Configuration

After reset the ADC is initialized for operation under control of the initialization control block. Initialization consists of five steps:

1) Serially shift programming data into the program shift register.

2) Decode the programming data and configure all circuits.

3) Perform eight DRAM wake-up cycles.

4) Initialize all of memory to zero with the proper check bits (ECC mode only).

5) Enable normal controller operation.

B. Service Request and Output Signal Generation

A parallel arbitration technique is used to minimize the delay from a port command, or a refresh request, to cycle start. With this technique a request is sent in parallel both to the arbiter and to the output signal generators. If the request channel was enabled by the arbiter prior to the request, then the request is serviced with no delay caused by arbitration. If the request channel was not enabled prior to the request, then the request is stored in the request register until such time that the arbiter can enable the channel. The arbiter is designed to

enable that channel over which a request is most likely to arrive next, so that, in general, a request is serviced without arbitration delay.

Characteristics of request rates in dual-port memories vary from application to application. Hence, the arbiter must be provided with some indication of what these characteristics are in order to be able to decide with a high probability of success which channel should be enabled during periods of inactivity. For this purpose, the arbiter may be programmed to enable a channel according to one of two prioritization rules: Port A Preferred or Most-Recently-Used Port preferred. With the former arbitration rule, requests are expected to arrive, in general, over channel A, irrespective of the recent history of requests, and, hence, this channel is enabled whenever there are no requests pending. With the latter arbitration rule, requests are expected to arrive in bursts from either port A or port B; and, hence, whichever channel was last serviced remains enabled until a request from another port arrives.

Parallel arbitration has a significant impact on a port sending back-to-back commands: with arbitration delay the bandwidth of the port would be significantly reduced, but with the requesting channel already enabled when a request arrives, no time is lost for arbitration between cycles.

Once a cycle starts, it runs to completion without further intervention of the requesting channel. The cycle timing control provides start and stop pulses for output signal generation.

C. Address Path

The address path is responsible for providing a multiplexed address to the DRAM from one of two sources: either the external microprocessor/bus or the internal refresh/scrub address counter. Timing is provided by the cycle timing control block.

IV. LOGIC AND CIRCUIT DESIGN

Several of the ADC design attributes are listed below.

Process—HMOSII
Die size—199 × 223 mil²
Number of devices—7 K
Package—68-pin JEDEC chip carrier
Supply voltage—+5 V
Supply current—400 mA
Logic sequence (clock) frequency—16 MHz
Clock duty cycle—24 to 68 percent
Capacitive drive capability: Address—550 pF; $\overline{RAS}$, $\overline{CAS}$—250 pF; All other outputs—150 pF
Command input setup time to clock for cycle start—20 ns
$\overline{RAS}$ output (i.e., cycle start) delay from clock—35 ns.

Several novel logic and circuit design techniques were used to achieve performance goals. Two of the performance goals, and the design techniques used to achieve them, are described below:

1) 16 MHz sequence frequency.
2) 20 ns setup time/35 ns delay time for cycle start.

A. 16 MHz Sequence Frequency

The ADC logic is sequenced using an *undivided* 16 MHz clock. This frequency is significantly higher than that used in other clocked chips implemented with technologies similar to HMOSII. To attain this frequency, three design techniques were used:

1) Single-edge logic.
2) Single-phase clocking.
3) Modular circuit design.

It was essential that the circuit design of an NMOS chip clocked at a frequency as high as 16 MHz be as immune as possible to variations in the clock parameters and, in particular, to variations in the clock waveshape. This requirement was met by designing circuitry that is very insensitive to clock duty cycle and to clock waveshape. To this end, all circuitry was implemented with single-edge logic using single-phase clocking. A modular circuit design methodology was also adopted in order to ensure consistent design standards throughout the chip.

1) Single-Edge Logic: Fig. 6 compares the timing of logic operations implemented with dual-edge logic and with single-edge logic. Dual-edge logic is characterized by operations performed in two nonoverlapping steps. Fig. 6 (a) illustrates dual-edge logic timing for the example of a register transfer operation over a precharged bus in a hypothetical microprocessor. During the portion of the clock period marked t_L the bus over which the transfer is to take place is precharged to a high voltage level. During the portion of the period marked t_H the contents of the first register are read out onto the bus and simultaneously written from the bus into the second register. The two parameters t_L and t_H are each specified with minimum values. These values translate into the minimum and maximum values of the clock duty cycle. In general, the requirements of t_L and t_H force the range of clock duty cycle values to be very narrow. Hence, dual-edge logic is usually very sensitive to clock duty cycle variations.

Fig. 6 (b) illustrates the timing of single-edge logic for the case of a sequential machine, in the form of which the ADC was designed. Single-edge logic is characterized by operations that start and end on only one of the clock edges. The second edge does not participate in such operations and, ideally, may occur at any point in the clock cycle. Thus, single-edge logic ideally can operate with a clock having a duty cycle ranging from 0 to 100 percent although, in practice, the attainable range is narrower. The ADC is specified to operate with a clock whose duty cycle ranges from 24 to 68 percent.

2) Single-Phase Clocking: Clocked NMOS logic is commonly sequenced using two nonoverlapping clock phases derived from the main clock [7]. This dual-phase clocking, while allowing for straightforward circuit design, is sensitive to clock-phase distortion. Fig. 7 illustrates the two detrimental effects of clock-phase distortion: phase overlap and dead time.

Phase distortion is the result of several factors, such as faulty clock-phase generator operation, RC delay in the path of one or both clock phases, or even ringing caused by LC loading. If the distortion takes the form of phase overlap, a fatal situation could result: during the overlap interval the sequential logic momentarily becomes combinatorial. In normal operation an information bit propagates through only one logic stage per clock period. If the propagation delay of a stage is less than the width of the overlap interval, the bit could propagate
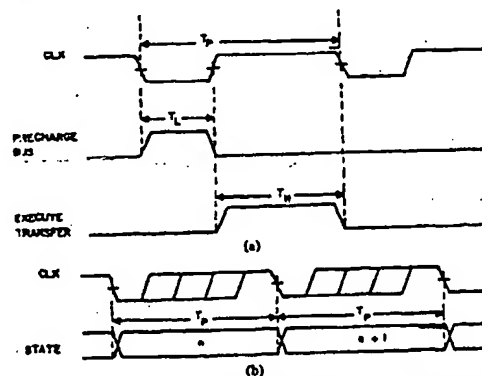
Fig. 6. Single-edge logic versus dual-edge logic. (a) Dual-edge logic timing. (b) Single-edge logic timing.
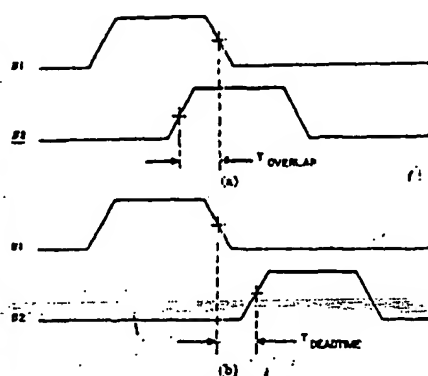
Fig. 7. Effects of clock-phase distortion. (a) Phase overlap. (b) Dead time.

through more than one stage and fatally corrupt the logic state of the chip.

Dead time, on the other hand, is not fatal, but it represents an interval during which logic propagation is suspended. Hence, dead time reduces the amount of time available for logic propagation and represents a design constraint.

A single-phase clocking scheme was chosen for the ADC in order to avoid both phase overlap and dead time. Fig. 8 (a) and 8 (b) compare the basic D-type flip-flop implemented with single-phase clocking, as used in the ADC, with a D-type flip-flop implemented with two-phase clocking. In the dual-phase implementation, the level at the input D is sampled on the rising edge of ϕ_1 and held on its falling edge, while the sampled level is transferred to output Q on the rising edge of ϕ_2. In the single-phase implementation, the level at input D is sampled on the rising edge of ϕ, while the level is simultaneously held and transferred to output Q on the falling edge of ϕ. Thus, unlike

in the dual-phase implementation, the hold and transfer operations in the single-phase implementation always occur *at the same point*. This characteristic of the single-phase implementation makes it highly insensitive to clock distortion: any shift in the hold point of the master caused by clock distortion will be tracked by a similar shift in the transfer point of the slave.

3) Modular Circuit Design: The logic and circuit design was done by a team of design engineers working independently on individual circuit blocks. A modular circuit design methodology was devised for standardizing design practices among the team members in order to ensure that blocks designed by different engineers would have compatible transient behavior.

Conceptually, most of the chip logic was partitioned into logic modules. A logic module is centered around a D-type flip-flop, so that a one-to-one correspondence exists between logic modules and D-type flip-flops. The output of a module is just the output of the module flip-flop, while the inputs to the module are either outputs from other modules or inputs external to the chip. Fig. 9 (a) illustrates a single logic module, while Fig. 9 (b) illustrates a hypothetical network of logic modules.

Signals coming out of blocks were assigned standard output delays of from 20 to 30 ns, while signals going into blocks were assigned standard input set-up times of from 15 to 35 ns. Thus, since the input and output timings of an individual module were well defined, the module could be designed as a self-contained unit with only a minimal reliance on knowledge of those modules to which it must interface. This methodology was an important factor in the achievement of full-functionality at 16 MHz on the very first iteration of the chip.

B. 20 ns Setup Time/35 ns Delay Time to Cycle Start

One of the most important performance requirements of the ADC is that a memory cycle start as soon as possible after the arrival of a command. Thus, in the case of a command from an enabled port, the memory cycle is required to start on the same clock edge that samples the command.

Starting a memory cycle involves triggering up to three out-
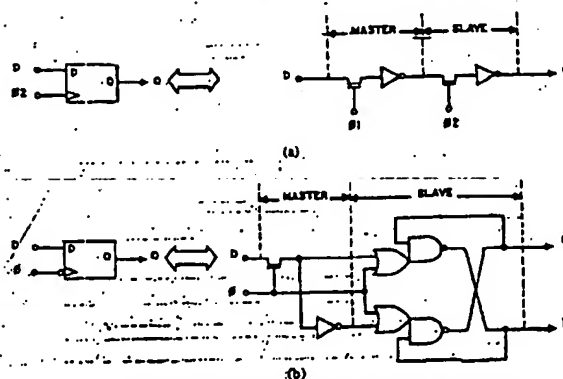
Fig. 8. D-type flip-flop implementation. (a) Dual-phase-clock implementation. (b) Single-phase-clock implementation.
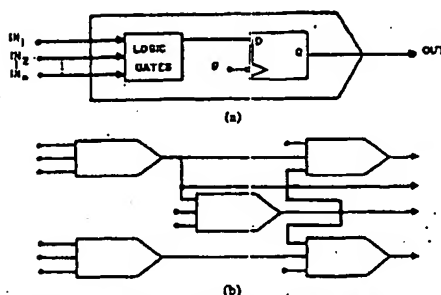
Fig. 9. Logic module. (a) Single module. (b) Network of modules.

put generators and another two internal circuit blocks. In terms of logic gates, up to approximately 150 gates, distributed throughout the chip, may have to sample a single external input signal and trigger operations on the same clock edge that sampled the input. The setup time requirement for such inputs is 20 ns maximum. The design problem posed by this requirement was how to bus the input signals throughout the chip to the target gates without incurring unacceptable delays en route.

To minimize delay in the paths from an input pad to all the gates qualified by the input, three techniques were used:

1) Low-resistance input protection devices.
2) Metal busing.
3) Local TTL-to-MOS buffering.

The scheme based on these techniques is illustrated in Fig. 10. The low-resistance input protection devices along with metal busing minimize the RC delay in the path from the pad to the target gates. The optimum low-resistance input protection device was found to be a variation on the common diffused-resistor/grounded-gate-transistor combination. The series resistance of the diffused resistor was reduced to an

acceptable level by increasing its width-to-length ratio, while the width of the grounded-gate transistor was increased proportionally in order to compensate for the lowered series resistance. Most of the critical input signals are bussed over the wide T-shaped bus appearing in the upper portion of the photomicrograph in Fig. 2. Because of the large number of gates driven by a single input, a single TTL-to-MOS buffer for the input would have suffered a large delay as a result of the large capacitive load it would have had to drive. Instead, the input signal is bused unbuffered to the target gates, where individual buffers are provided at the entry points. Although this technique requires many buffers for each input signal, it contributes to a reduction of up to 10 ns in setup time.

The output delay time for the outputs qualified by these inputs is 35 ns maximum. Meeting this requirement was complicated by the fact that an output signal had to be triggerable off of either clock edge, depending on the configuration of the ADC. The circuit illustrated in Fig. 11 meets both requirements. It is essentially a synchronous RS-type flip-flop triggerable off of either clock edge, as determined by the signal RISE/FALL. Since ϕ is just the buffered CLK signal, it is delayed with respect to CLK. By triggering the circuit with CLK instead of with ϕ, up to 5 ns are saved from the overall delay time. A significant amount of overlap does exist between CLK and ϕ, but since the circuit does not interface with any other on-chip modules, the overlap is nonfatal. Note the local low-voltage source V_{LL} composed of an inverter tied to V_{CC} and a capacitor-connected transistor. V_{LL} provides a voltage level of about one enhancement-mode transistor threshold for the network of transmission gates during discharge of the storage nodes. Were the transmission gates connected directly to V_{SS}, their gate-to-source voltage would be approximately one threshold and they would leak off charge stored on the storage nodes. The capacitor-connected transistor acts as a decoupling capacitor and prevents V_{LL} from changing during discharge of the storage nodes.
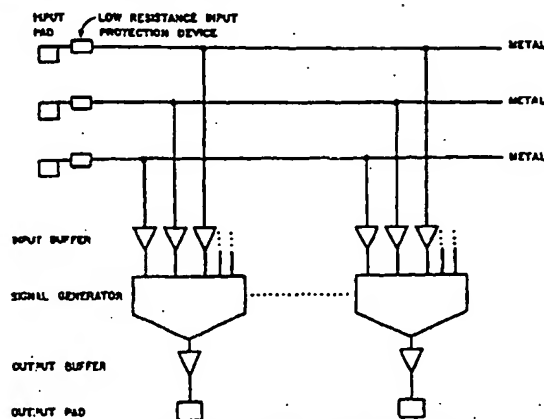
Fig. 10. Input signal busing technique for minimum delay en route.

SIGNALS
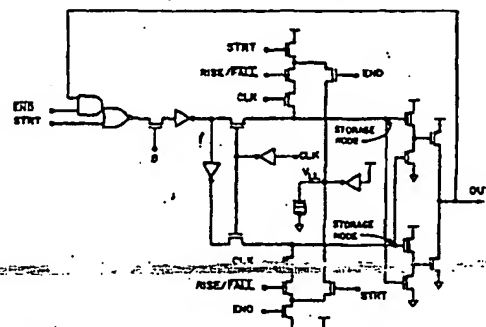
CLK - EXTERNAL CLOCK.
∅ - INTERNAL CLOCK (DERIVED FROM CLK)
STRT - START PULSE
DIO - DIO PULSE
RISE/FALL - CLOCK TRIGGER EDGE (STATIC SIGNAL)
OUT - OUTPUT (TO OUTPUT BUFFER)

(a)

(b)
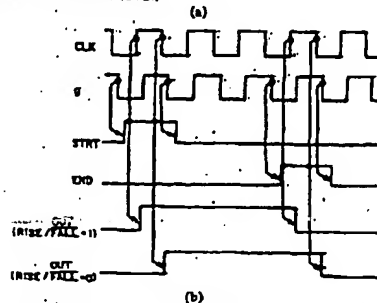
Fig. 11. Output generator. (a) Schematic diagram. (b) Timing.

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An Evaluation of Directory Schemes for Cache Coherence

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Abstract

The problem of cache coherence in shared-memory multiprocessors has been addressed using two basic approaches: directory schemes and snoopy cache schemes. Directory schemes have been given less attention in the past several years, while snoopy cache methods have become extremely popular. Directory schemes for cache coherence are potentially attractive in large multiprocessor systems that are beyond the scaling limits of the snoopy cache schemes. Slight modifications to directory schemes can make them competitive in performance with snoopy cache schemes for small multiprocessors. Trace driven simulation, using data collected from several real multiprocessor applications, is used to compare the performance of standard directory schemes, modifications to these schemes, and snoopy cache protocols.

1 Introduction

In the past several years, shared-memory multiprocessors have gained wide-spread attention due to the simplicity of the shared-memory parallel programming model. However, allowing the processors to share memory complicates the design of the memory hierarchy. The most prominent example of this is the *cache coherency* or *cache consistency* problem, which is introduced if the system includes caches for each processor. A system of caches is said to be *coherent* if all copies of a main memory location in multiple caches remain consistent when the contents of that memory location are modified [1]. A *cache coherency protocol* is the mechanism by which the coherency of the caches is maintained. Maintaining coherency entails taking special action when one processor writes to a block of data that exists in other caches. The data in the other caches, which is now stale, must be either invalidated or updated with the new value, depending on the protocol. Similarly, if a read miss occurs on a shared data item and memory has not been updated with the most recent value (as would happen in a copy-back cache), that most recent value must be found and supplied to the cache that missed. These two actions are the essence of all cache coherency protocols. The protocols differ primarily in how they determine whether the block is shared, how they find out where block copies reside, and how they invalidate or update copies.

Most of the consistency schemes that have been or are being implemented in multiprocessors are called *snoopy cache* protocols [2,3,4,5,6,7] because each cache in the system must watch all coherency transactions to determine when consistency-related actions should take place for shared data. Snoopy cache schemes store the state of each block of cached

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data in the cache directories – the information about the state of the cached data is distributed.

Another class of coherency protocols is *directory-based* [8,9,10,11]. Directory-based protocols keep a separate directory associated with main memory that stores the state of each block of main memory. Each entry in this centralized directory may contain several fields depending on the protocol, for example, a dirty bit, a bit indicating whether or not the block is cached, pointers to the caches that contain the block, etc.

How do snoopy cache protocols work? A typical scheme enforces consistency by allowing multiple readers but only one writer. The state associated with a block's cached copy denotes whether the block is, for example, (i) invalid, (ii) valid (possibly shared), or (iii) dirty (exclusive copy). When a cache miss occurs, the address is broadcast on the shared bus. If another cache has the block in state dirty, the state is changed to valid and the block is supplied to the requesting cache. In addition, for write misses all copies of the block are invalidated. Similarly, on a write bit to a clean block, the address is broadcast and each cache must invalidate its copy. In general, all cache transactions that may require a data transfer or state change in other caches must be broadcast over the bus.

Snoopy cache schemes are popular because small-scale multiprocessors can live within the bandwidth constraints imposed by a single, shared bus to memory. This shared bus makes the implementation of the broadcast actions straightforward. However, snoopy cache schemes will not scale beyond the range of the number of processors that can be accommodated on a bus (probably no more than 20). Attempts to scale them by replacing the bus with a higher-bandwidth communication network will not be successful since the consistency protocol relies on low-latency broadcasts to maintain coherency. For this reason, shared-memory multiprocessors with large numbers of processors, such as the RP3 [12], do not provide cache coherency support in hardware.

These snoopy cache schemes also interfere with the processor-cache connection. Because the caches of all processors are examined on each coherency transaction, interference between the processor and its cache is unavoidable. This interference can be reduced by duplicating the tags and snooping on the duplicate tags. However, the processor must write both sets of tags and thus arbitration is required on the duplicate tags. This impacts the cache write time which may slow down the overall cycle time, especially in a high performance machine. Attempts to reduce the bus traffic generated by cache coherency requests in a snoopy cache scheme results in fairly complex protocols. These may impact either the cache access time or the coherency transaction time.

In this paper we propose that directory-based schemes are better suited to building large-scale, cache-coherent multi-

processors, where a single bus is u... able for a communication mechanism. This paper is a first step in evaluating directory schemes using traces from real multiprocess applications. Although we do not have sufficient data to demonstrate quantitatively that the directory schemes are effective in a large-scale multiprocessor, we do discuss how these directory schemes can be scaled and we demonstrate that their performance in a small-scale multiprocessor is acceptable.

We use trace-driven simulation, with traces obtained from real multiprocessor applications, to evaluate a basic directory-based coherency protocol that uses bus broadcasts and verify that its performance approaches that of snoopy cache schemes. We then obviate broadcasts by including a valid bit per cache in each directory entry, allowing sequential invalidation of multiple cached copies. Performance is not significantly degraded by this modification, and in most cases (over 45% of writes to previously-clean blocks) no more than one sequential invalidation request is necessary. Unfortunately, the need for a valid bit per cache restricts the ability to add on to an existing multiprocessor without modifying parts of the existing system. This motivates a scheme that can perform up to some small number of sequential invalidates to handle the most frequent case, and that resorts to some form of "limited broadcast" otherwise.

The paper first reviews previous directory schemes and discusses how they overcome the limitations created by snoopy cache schemes. It also proposes a general classification of these techniques, and identifies a few that seem most interesting for performance and implementation reasons. Section 3 outlines the schemes that we evaluate. We describe our evaluation method and the characteristics of our multiprocessor address traces in Section 4. Section 5 evaluates basic directory and snoopy cache schemes and discusses their performance. Section 6 then extends the discussion to include more scalable directory protocols, and Section 7 concludes the paper.

2 Directory Schemes for Cache Consistency

The major problems that snoopy cache schemes possess are limited scalability and interference with the processor-cache write path. How do directory schemes address these problems? The major advantage directory schemes have over snooping protocols is that the location of the caches that have a copy of a shared data item are known. This means that a broadcast is not required to find all the shared copies. Instead, individual messages can be sent to the caches with copies when an invalidate occurs. Since these messages are directed (i.e., not broadcast), they can be easily sent over any arbitrary interconnection network, as opposed to just a bus. The absence of broadcasts eliminates the major limitation on scaling cache coherent multiprocessors to a large number of processors.

Because we no longer need to examine every cache for a copy of the data, the duplicate tags can be eliminated. Instead, we store pointers in main memory to the caches where the data is known to reside and invalidate their copies. The protocols are also simpler than the distributed snoopy algorithms because of the centralization of the information about each datum.

Several directory-based consistency schemes have been pro-

posed in the literat... Tang's method [5] allows clean blocks to exist in many c... .es, but disallows dirty blocks from residing in more than one cache (most snoopy cache coherency schemes use the same policy). In this scheme, each cache maintains a dirty bit for each of its blocks, and the central directory kept at memory contains a copy of all the tags and dirty bits in each cache. On a read miss, the central directory is checked to see if the block is dirty in another cache. If so, consistency is maintained by copying the dirty block back to memory before supplying the data; if the directory indicates the data is not dirty in another cache, then it supplies the data from memory. The directory is then updated to indicate that the requesting cache now has a clean copy of the data. The central directory is also checked on a write miss. In this case, if the block is dirty in another cache then the block is first flushed from that cache back to memory before supplying the data; if the block is clean in other caches then it is invalidated in those caches (i.e., removed from the caches). The data is then supplied to the requesting cache and the directory modified to show that the cache has a dirty copy of the block. On a write hit, the cache's dirty bit is checked. If the block is already dirty, there is no need to check the central directory, so the write can proceed immediately. If the block is clean, then the cache notifies the central directory, which must invalidate the block in all of the other caches where it resides.

Censier and Feautrier [9] proposed a similar consistency mechanism that performs the same actions as the Tang scheme but organises the central directory differently. Tang duplicates each of the individual cache directories as his main directory. To find out which caches contain a block, Tang's scheme must search each of these duplicate directories. In the Censier and Feautrier central directory, a dirty bit and a number of valid (or "present") bits equal to the number of caches are associated with each block in main memory. This organization provides the same information as the duplicate cache directory method but allows this information to be accessed directly using the address supplied to the central directory by the requesting cache. Each valid bit is set if the corresponding cache contains a valid copy of the block. Since a dirty block can only exist in at most one cache, no more than one of a block's valid bits may be set if the dirty bit is set.

Yen and Fu suggest a small refinement [11] to the Censier and Feautrier consistency technique. The central directory is unchanged, but in addition to the valid and dirty bits, a flag called the single bit is associated with each block in the caches. A cache block's single bit is set if and only if that cache is the only one in the system that contains the block. This saves having to complete a directory access before writing to a clean block that is not cached elsewhere. The major drawback of this scheme is that extra bus bandwidth is consumed to keep the single bits updated in all the caches. Thus, the scheme saves central directory accesses, but does not reduce the number of bus accesses versus the Censier and Feautrier protocol.

Archibald and Baer present a directory-based consistency mechanism [10] with a different organization for the central directory that reduces the amount of storage space in the directory, and also makes it easier to add more caches to the system. The directory saves only two bits with each block in main memory. These bits encode one of four possible states: block not cached, block clean in exactly one cache, block clean in an unknown number of caches, and block dirty in exactly one cache. The directory therefore contains no information

to indicate which caches contain a block; the scheme relies on broadcasts to perform invalidates and write-back requests. The block clean in exactly one cache state obviates the need for a broadcast when writing to a clean block that is not contained in any other caches.

Two clear differences are present among these directory schemes: the number of processor indices contained in the directories and the presence of a broadcast bit. We can thus classify the schemes as $Dir_i X$, where i is the number of indices kept in the directory and X is either B or NB for Broadcast or No Broadcast. In a no-broadcast scheme the number of processors that have copies of a datum must always be less than or equal to i, the number of indices kept in the directory. If the scheme allows broadcast then the numbers of processors can be larger and when it is (indicated by a bit in the directory) a broadcast is used to invalidate the cached data. The one case that does not make sense is $Dir_n NB$, since there is no way to obtain exclusive access.

In this terminology, the Tang scheme is classified as $Dir_n NB$, the Censier and Feautrier scheme is $Dir_n NB$ also, and the Baer and Archibald scheme is $Dir_n B$. Our evaluation concentrates on a couple of key points in the design space: $Dir_i NB$ and $Dir_n B$. We will also present results for $Dir_n NB$.

There are two potential difficulties that prevent scalability of the directory schemes. First, if the scheme always or frequently requires broadcast, then it will do no better than the snoopy schemes. Variations in the directory schemes (e.g., increasing the value of i in a $Dir_i B$ scheme) decrease the frequency of broadcast. We must also examine the dynamic numbers of caches that contain a shared datum to evaluate the actual frequency of occurrence. Second, the access to the directory is a potential bottleneck. However, we will show that the directory is not much more of a bottleneck than main memory, and the bandwidth to both can be increased by having a distributed memory hierarchy rather than centralized. That is, memory is distributed together with individual processors. In addition to certain advantages in providing scalable bandwidth to the memories from the local processor, the organization distributes the directory, associating it with the individual memory modules.

3 Schemes Evaluated

We will evaluate two directory schemes (called $Dir_i NB$ and $Dir_n B$), and two snoopy cache schemes (Write-Through-With-Invalidate and Dragon) for comparison purposes. These particular snoopy cache techniques were selected because they represent two extremes of performance and complexity. The two directory schemes are also extremes in the number of simultaneous cached copies allowed. The following is a description of these four protocols.

The most restrictive of the four schemes is $Dir_i NB$ in that a given block is allowed to reside in no more than one cache at a time; therefore, there can be no data inconsistency across caches. The directory entry for each block consists of a pointer to the cache that contains the block. On a cache miss, the directory is accessed to find out which cache contains the block, that cache is notified to invalidate the block and write it back to memory if dirty, and the data is then supplied to the requesting cache. $Dir_i NB$ is included in the evaluation because it is perhaps the simplest directory-based consistency scheme and is easily scaled to support a large

number of processors.

The $Dir_n B$ is the Archibald and Baer scheme [10] outlined in the previous section. Like many consistency protocols, a clean block may reside in many caches, while a dirty block may exist in exactly one cache. Invalidations are accomplished with broadcasts; a similar scheme that uses sequential invalidates in place of broadcasts ($Dir_n NB$) will later be shown to have nearly the same performance. For the initial evaluation, broadcasts are used in both the directory and snooping schemes because it results in a simpler cost model and allows a fair comparison of the two.

Write-Through-With-Invalidate (WTI) is a simple snoopy cache protocol that relies on a write-through (as opposed to copy-back) cache policy and is used in several commercial multiprocessors. All writes to cache blocks are transmitted to main memory. Other caches snooping on the bus check to see if they have the block that is being written; if so, they invalidate that block in their own cache. When a different processor accesses the block, a cache miss will occur and the current data will be read from memory. Like $Dir_n B$, multiple cached copies of clean blocks can exist simultaneously. Because of the high level of bus traffic caused by the write-through strategy, WTI is generally considered to be one of the lowest-performance snooping cache consistency protocols.

While the three previous schemes are all invalidation protocols, Dragon is an update protocol, i.e., it maintains consistency by updating stale cached data with the new value rather than by invalidating the stale data [13]. The cache keeps state with each block to indicate whether or not each block is shared; all writes to shared blocks must be broadcast on the bus so that the other copies can be updated. Dragon uses a special "shared" line to determine whether a block is currently being shared or not. Each cache snoops on the bus and pulls the shared line whenever it sees an address for which it has a cached copy of the data. Dragon is often considered to have the best performance among snoopy cache schemes.

4 Evaluation Methodology

Simulation using multiprocessor address traces is our method of evaluation. Most previous studies that evaluated directory schemes used analytical models [14,9] and those that used simulation had to make rough assumptions about the characteristics of shared memory references [10]. Because the performance of cache coherence schemes is very sensitive to the shared-memory reference patterns, both of these previous methods have the drawback that the results are highly dependent on the assumptions made. Trace-driven simulation has the drawback that the same trace is used to evaluate all consistency protocols, while in reality the reference pattern would be different for each of the schemes due to their timing differences. But the traces represent at least one possible run of a real program, and can accurately distinguish the performance of various schemes for that run.

This paper deals with the inherent cost of sharing in multiprocessors and the memory traffic required to maintain cache consistency. We therefore exclude the misses caused by the first reference to a block in the trace because these occur in a uniprocessor infinite cache as well. The additional overhead due to multiprocessing now consists of (i) the extra misses that occur due to fetching the block into multiple caches and (ii) the cache consistency-related operations. Our results represent exactly this overhead.

We wish to isolate and measure only the traffic incurred in maintaining a coherent shared memory system in a multiprocessor. To this end our simulations use infinite caches to eliminate the traffic caused by interference in finite caches. The performance of an infinite cache is also a good approximation to that of a very large cache, where the miss rate is essentially the cost of first-time fetches. Moreover, the performance of a system with smaller caches can be estimated to first order by adding the costs due to the finite cache size. Typical cache miss rates are reported in [15,16].

4.1 Performance Measures

To determine the absolute performance of a multiprocessor system using total processor utilizations, a simulation must be carried out for every hardware model desired. A problem with this approach is that the sharing characteristics may change because the simulation model is different from the hardware used for gathering data.

We would like a metric for performance that is not tied to any particular processor or interconnection network architecture. We use the communication cost per memory reference as our basic metric. This cost is simply the average number of cycles that the bus (or network) is busy during a data transfer from a cache to another cache, cache to directory, and from cache to or from main memory. We refer to this metric simply as bus cycles per memory reference. This metric abstracts away details of how the directories are implemented, either as centralized or distributed. It also requires no assumptions about the relative speeds of local and non-local memories, local and non-local buses, or processor and the bus.

Since the snoopy cache schemes require a bus-based architecture, we often talk of a bus in our directory models. However, the directory schemes we discuss are general enough to work in any network architecture. While the bus cycles metric allows us to compare the relative merits of various cache consistency schemes, it cannot indicate accurately the absolute performance of a multiprocessor. However, in lightly loaded systems, multiprocessor performance could still be approximated to first order from the number of bus cycles used per memory reference.

The bus cycles per reference for a given cache consistency scheme are computed as follows. First we measure event frequencies for various schemes by simulating multiple infinite caches, where events are different types of memory references. The simulator reads a reference from a trace and takes a set of actions depending on the type of the reference, the state of the referenced block, and the given cache consistency protocol.

The event frequencies are now weighted by their respective costs in bus cycles to give the aggregate number of bus cycles used per reference. For example, a cache miss event might require 5 bus cycles of communication cost (1 cycle to send the address, and 4 cycles to get 4 words of data back). If the rate of cache misses is, say, 1%, then the bus cycles used up by cache misses per reference is 0.05. In like manner, the costs due to other events are added to get the aggregate cost per reference. Since the choice of the hardware model (i.e., cost per event) is independent of the event frequencies, we need just one simulation run per protocol to compute the event frequencies, and we can then vary costs for different hardware models.

Details of traces used in simulations are given in Section 4.4. The block size used throughout this paper is 4 words (16 bytes). In all schemes we assume that instructions do not cause any cache consistency related traffic. In addition, we do not include the bus traffic caused by instruction misses in our performance estimations.

4.2 Event Frequencies

The event types of interest in a particular scheme are those that may result in a bus transaction. All the schemes require the frequency of read and write misses (read-miss or rm and write-miss or wm. Depending on the scheme some other events ???? are also needed:

- The Dragon events include the fraction of references to blocks that are clean or dirty in another cache on a read or write miss (rm-blk-cln, rm-blk-drty, wm-blk-cln, and wm-blk-drty). The clean and dirty numbers indicate when a block is supplied by another cache as opposed to from main memory. In addition, we need the frequency of write updates to blocks present in multiple caches on a write hit (wh-distrib).

- The write-through scheme requires the frequency of writes (write) because all writes are transmitted to main memory.

- In the Dir_iNB scheme, we need the fractions of read and write references that miss in the cache, but are present in a dirty or clean state in another cache (rm-blk-cln, rm-blk-drty, wm-blk-cln, and wm-blk-drty). These events indicate when invalidation requests must be sent to another cache and when dirty blocks have to be written back to main memory.

- In the Dir_iB scheme, in addition to the four events for the Dir_iNB scheme, we need the proportion of write hits to a clean block (wh-blk-cln). This event represents queries to the directory to check whether the block resides in any other cache and has to be invalidated. We also measure the distribution of the number of caches the block resides in during a possible invalidation situation to determine the impact of various invalidation methods. The various invalidation methods include full broadcast, limited broadcast, and sequential invalidation messages to each cache.

4.3 Bus Models

The bus cycle costs for the various events depend on the sophistication of the bus and main memory. The examples given in this paper use the bus timing depicted in Table 1. From this basic bus model, and some assumptions about the sophistication of the bus, we can estimate the cost in bus cycles for each of the events that cause bus traffic. Because the costs can differ depending on the type of bus or interconnection network used, we will use two bus types of widely diverse complexity to give an idea of how the schemes will perform over a range of bus and memory organizations. On the sophisticated end of the spectrum, we use a pipelined bus model that has separate data and address paths. At the other end we use a non-pipelined bus that has to multiplex the address and data on the same bus lines. The data transfer width of both buses is assumed to be one word (32 bits).

For the pipelined bus with separate lines for address and data, memory or non-local cache accesses cost 5 cycles (1

Bus Operation	Bus Cycles
Send address	1
Transfer 1 data word	1
Invalidate	1
Wait for Directory	2
Wait for Memory	2
Wait for Cache	3

Table 2: Summary of bus cycle costs.

Access Type	Pipelined Bus	Non-Pipelined Bus
mem access	5	7
cache access	5	6
write back	4	4
invalidate	1	1
wt or wup	1	2
dir access	1	3

cycle to send the address and 4 cycles to get the data). The bus is not held during the access. Write-backs cost 4 cycles: the first cycle sends the address and the first data word; the remaining 3 words are sent in the next three cycles. When the data is transferred to memory during a write-back, the requesting cache also receives it. The bus cycles used for data transfer are then counted under the write-back category. A write-through to memory or a write update to another cache is 1 cycle. A directory check uses 1 cycle to send the address, and invalidates are also 1 cycle.

In the non-pipelined bus model, the bus has to be held during the memory or non-local cache access. Here a memory access costs 7 cycles, 1 cycle to send the address, 2 cycles to wait for the memory access, and 4 cycles to get the data. An access from another cache is 6 cycles, and takes a cycle less than the memory access because the cache access wait is only one cycle. Write-backs still cost 4 cycles; the waiting for memory is counted under the memory access category, and the bus need not be held while the write into memory is taking place. As in the pipelined bus, the data is also received by the requesting cache on a write-back. A write-through or a write update to another cache is 2 cycles, 1 cycle to send the address and 1 cycle to send the data word. A directory check is 3 cycles, 1 cycle to send the address and 2 cycles to access the directory. When possible the directory access is overlapped with memory access. Invalidations cost 1 cycle. These costs for the pipelined and non-pipelined bus models are summarized in Table 2.

In the non-pipelined bus, once the address and the data have been sent to memory or to another cache on a write (or write-back) operation we assume that the bus need not be held while data is being written into memory. This is a simplifying assumption and is usually true if memory is interleaved. We also assume that broadcast invalidates, like a single invalidate, take 1 cycle. We do not attempt to model the impact of broadcast invalidate on the bus cycle time.

4.4 Multiprocessor Trace Data

The traces used for simulation are obtained using a multiprocessor extension of the ATUM address tracing scheme [17]. The multiprocessor used for tracing was a VAX 8350 with

Trace	Refs	Inst	Dlid	DWri	User	Sys
POPS	3142	1624	1257	261	2917	325
THOR	3222	1456	1398	368	2727	493
PERO	3508	1834	1266	409	3242	266

four processors. An address trace contains interleaved address streams of the four processors. CPU numbers and process identifiers of the active processes are also included in the trace so that any address in the trace can be identified as coming from a given CPU and given process. A current limitation of ATUM traces is that only four-CPU traces can be obtained. We are currently developing a multiprocessor simulator that builds on top of the VAX T-bit mechanism and can provide accurate simulated traces of a much larger number of processors.

The traces show some amount of sharing between processors that is induced solely by process migration. The characteristics of migration-induced sharing is significantly different from sharing present in the application processes [18]. We would like to exclude this form of sharing from our study since a large multiprocessor would probably try to minimize process migration. Therefore, for this study, we consider sharing between processes (as opposed to sharing between processors), which means that a block is considered shared only if it is accessed by more than one process. Because the time sequence of the references in the trace is strictly maintained, the temporal ordering of various synchronization activities in the trace, such as getting or releasing a synchronization lock, is still retained. As a check on this model, we collected all our statistics based on both process sharing and processor sharing and found that the numbers were not significantly different. The similarity is due to the few instances of process migration in our traces.

We currently use three traces for this study. The traces are of parallel applications running under the MACH operating system [19]. Table 3 describes the characteristics of the traces used for this study. POPS [20] is a parallel implementation of OPS5, which is a rule-based programming language. THOR is a parallel implementation of a logic simulator done by Larry Soule at Stanford University. PERO is a parallel VLSI router written by Jonathan Rose at Stanford. All traces include operating system activity, which comprises roughly 10% of the traces.

The traces show a larger-than-usual read-to-write reference ratio due to spins on locks in POPS and THOR. The spins correspond to the first test in a test-and-test-&-set synchronization primitive. These appear as reads of a data word. Roughly one-third of all the reads correspond to reads due to spinning on a lock. We will look at how the number of spins on a lock affect the performance of cache consistency schemes in Section 5.2. The ratio of reads to writes in PERO is also high, but this reference behavior is a result of the algorithm used in the program.

5 Evaluation of Directory-Based and Snoopy-Cache Protocols

The first step in evaluating the four consistency schemes is to measure the frequency of each type of reference. Table 4 gives a breakdown of the various types of references that take place in the four schemes and their relative frequencies, averaged across the three traces. All numbers in this table are shown as a percentage of the total number of references.

Table 4: Event frequencies. The numbers are shown as a percentage of all references. The fractions in each subcategory add up.

Event Type	Schemes			
	$Dir_1 NB$	WTI	$Dir_0 B$	Dragon
instr	49.72	49.72	49.72	49.72
read	39.82	39.82	39.82	39.82
rd-hit	34.32	38.88	38.88	39.20
rd-miss(rm)	5.18	0.62	0.62	0.30
rm-blk-cln	4.78	-	0.23	0.14
rm-blk-drty	0.40	-	0.40	0.17
rm-first-ref	0.32	0.32	0.32	0.32
write	10.46	10.46	10.46	10.46
wrt-hit(wh)	10.19	10.25	10.35	10.36
wh-blk-cln	-	-	0.41	-
wh-blk-drty	-	-	9.84	-
wh-distrib	-	-	-	1.74
wh-local	-	-	-	8.62
wrt-miss(wm)	0.17	0.12	0.11	0.02
wm-blk-cln	0.08	-	0.02	0.01
wm-blk-drty	0.09	-	0.09	0.01
wm-first-ref	0.08	0.08	0.08	0.08

LEGEND

instr	Instructions
read	Reads
rd-hit	Read hits
rd-miss(rm)	Read misses
rm-blk-cln	Read miss, blk clean in another cache
rm-blk-drty	Read miss, blk dirty in another cache
rm-first-ref	Read miss, first reference to the blk
write	Writes
wrt-hit(wh)	Write hits
wh-blk-cln	Write hit, blk clean in the same cache
wh-blk-drty	Write hit, blk dirty in the same cache
wh-distrib	Write hit, block also in another cache
wh-local	Write hit, blk not in another cache
wrt-miss(wm)	Write miss
wm-blk-cln	Write miss, blk clean in another cache
wm-blk-drty	Write miss, blk dirty in another cache
wm-first-ref	Write miss, first reference to the blk

We can make several useful observations about the cache behavior as well as the data sharing behavior of the traces from these event counts. The most obvious feature of the numbers for the $Dir_1 NB$ consistency scheme is the high rate of data read misses (5.18% of all references), indicating a high penalty for allowing a block to reside in no more than one cache at a time. The $Dir_1 NB$ numbers also show a low rate of data write misses (0.17% of all references), which implies that most data writes occur on blocks which have first been

brought into the cache via read misses. Furthermore, it is usually the case that no other process accesses those blocks between the read immediately preceding a write and the write itself, since this situation would result in a write miss for the $Dir_1 NB$ scheme. The $Dir_0 B$ consistency technique, on the other hand, shows a much smaller rate of read misses (0.62%) than $Dir_1 NB$, illustrating that most of the misses incurred in $Dir_1 NB$ were caused by read sharing among multiple processes.

The fact that the reference rates for the WTI method match those of $Dir_0 B$ brings up an interesting point. A cache consistency protocol can be thought of as being made up of two parts: a specification of the state changes of the data in the caches (e.g., when is data brought into the cache, invalidated) and the protocol which is used to accomplish that specification (e.g., write-through with bus snooping, centralized directory). The frequency with which each of the events listed in Table 4 occurs depends only on the state change specification, not on the method used to implement it. Since $Dir_0 B$ and WTI both rely on the same basic data state-change model of allowing multiple cached copies of clean blocks but only a single copy of dirty blocks, their event frequencies are identical. (However, they do differ in that $Dir_0 B$ allows main memory blocks to become stale with respect to cache blocks. This distinction and the difference in cost associated with some events accounts for their disparity in performance.) This basic state-change model is also found in some other consistency schemes [7] and the event frequencies for $Dir_0 B$ and WTI are valid for these as well.

The Dragon consistency mechanism differs from the others in Table 4 because it is an update protocol rather than an invalidation protocol. For this reason the miss rates are very small in an infinite cache: once a block is loaded into a cache, it remains there forever. The most important events for Dragon are not cache misses, but rather write hits that cause a bus transaction. The numbers in the table indicate that roughly one-sixth of all writes require a bus broadcast to perform a write update.

Viewing the event frequencies in absolute terms (rather than in relation to the frequencies in other schemes) can provide some insight into the amount of overhead generated by enforcing cache consistency in a multiprocessor. One simple metric of this overhead (for an invalidation protocol) is the increase in the cache miss rate due to the invalidations required to ensure consistency. Since they were generated using infinite caches, the miss rates in Table 4 are an upper bound on the amount by which the miss rate of a finite-sized cache will increase.[2] From Table 4 we can compute the component of the miss rate due to invalidations caused by cache coherency. Because there are no invalidations in the Dragon scheme, its miss rate is the native miss rate for these traces. From Table 4, the data component of the native miss rate is 0.72%. Therefore, the difference between the $Dir_0 B$ data miss rate and the native data miss rate is $1.13 - 0.72 = 0.41\%$ which is the miss rate component due to cache coherency. Consistency-related misses therefore comprise $0.41/1.13 = 36\%$ of the total miss rate.

In invalidation schemes like $Dir_0 B$, a write to a previously-

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[1] Accesses to lock variables – a successful test followed by a test and set in the test-and-test-&-set primitive – are an example.

[2] The coherency-related misses will be lower in a finite-sized cache because some of the blocks that would be invalidated to enforce consistency in an infinite cache have already been purged in a finite cache due to cache interference.
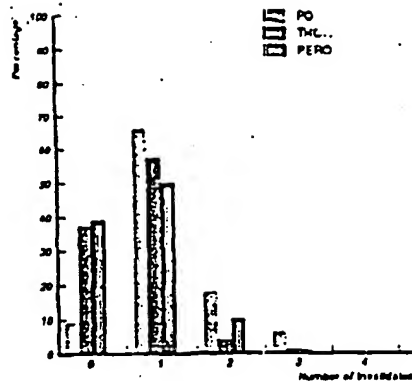
Figure 1: Number of caches in which a block must be invalidated on a write to a previously-clean block.

Figure 2: Range of bus cycle requirements (average). The low value of each bar corresponds to the pipelined bus and high value to the non-pipelined bus.

clean block must invalidate that block in all other caches that have a copy. This is the case for two events in Table 4: *wm-blk-cln* and *wh-blk-cln*. Figure 1 shows the histogram of the number of other caches that contain a previously-clean block when it is written (i.e., when one of the above two events occurs). This number is equal to the number of caches in which a clean block must be invalidated when it is written. The figure shows that on average, over 85% of the writes to previously-clean blocks cause invalidations in no more than one cache.[2] This points out the inefficiency in using a bus broadcast to accomplish the invalidation operation, and suggests some possible enhancements to directory-based consistency schemes which will be discussed shortly.

Figure 2 shows the average number of bus cycles per reference, calculated as described in Section 4. The two endpoints of each bar represent the performance of the pipelined and non-pipelined buses. The performance of Dir_0B approaches that of the Dragon scheme for this metric. Not surprisingly, Dir_1NB and WTI are much worse than Dir_0B and Dragon. As observed in [1], Dragon shows the best performance because the cost of a write update is assumed to be much lower than the cost of an invalidation and a subsequent miss. Figure 3 shows the average number of bus cycles per reference for the individual traces. The numbers for the POPS and THOR traces are similar, while those for PERO are much smaller. The chief reason is that the fraction of references to shared blocks in PERO is much smaller than in POPS and THOR. Another observation is that the relative performance of the four schemes does not depend strongly on the sophistication of the bus. For the remainder of the paper we will focus on the pipelined bus for brevity.

Table 5 shows the breakdown by operation of the average number of bus cycles per reference. Dir_0B is shown to use

[2] The number of times that invalidations occur in no more than one cache, computed as a fraction of all references that may require invalidations, is even larger. Such references, in addition to writes that occur to previously-clean blocks, include read/write misses to blocks dirty in another cache (*rm-blk-drty*, *wm-blk-drty*), which require exactly one invalidation.
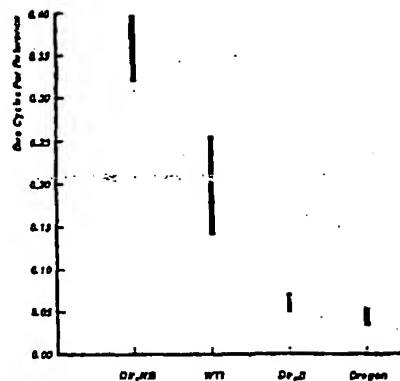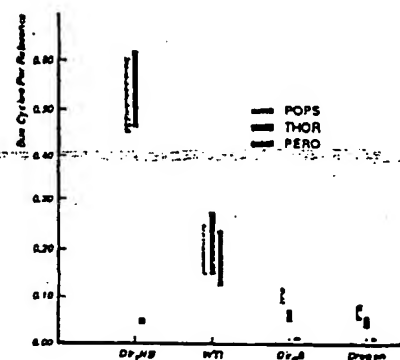
Figure 3: Range of bus cycle requirements for the individual traces. The low value of each bar corresponds to the pipelined bus and high value to the non-pipelined bus.

versus 0.0336). The performance of Dir_0B in a real system is closer to Dragon than this metric i ...tes because the fixed costs of references which use the bus impact Dragon more severely, as pointed out in Section 5.1.

As an interesting aside, the Dir_0B event frequencies can be used to estimate the performance of the Berkeley Ownership protocol [7] by modifying the Dir_0B cost model. The cost models are different because Dir_0B has to probe the directory to find out whether it needs to do an invalidate, while the Berkeley scheme gets this information from the state of the block in the cache.[4] The cost model for the Berkeley scheme is thus derived from the Dir_0B scheme by trivially setting the directory access cost to 0 bus cycles. With this model, the number of bus cycles consumed by an average reference in the Berkeley scheme is 0.0409, placing it roughly midway between the Dir_0B and Dragon schemes.

Table 5: Breakdown of bus cycles for the pipelined bus. The category "wt or wup" stands for write-through in the WTI scheme and write update in the Dragon scheme. Note that directory accesses can always be overlapped with memory accesses in Dir_1NB.

Access	Schemes			
Type	Dir_1NB	WTI	Dir_0B	Dragon
mem access	0.2479	0.0369	0.0173	0.0160
write back	0.0196	-	0.0196	-
invalidate	0.0535	-	0.0081	-
wt or wup	-	0.1037	-	0.0176
dir access	-	-	0.0041	-
cumulative	0.3210	0.1406	0.0491	0.0336

The data in Table 5 is shown graphically in Figure 4. The figure depicts the breakdown of the bus cycles as a fraction of the total number of bus cycles used by each scheme, highlighting the relative importance of various events. In Dir_1NB, for instance, the high miss rate on clean blocks makes the number of bus cycles spent on invalidations and write-backs small compared to the number of memory accesses. Not surprisingly, most of the bus cycles consumed in WTI are due to the write-through cache policy. The Dragon scheme splits its bus cycles evenly between loading up each cache with data and using the bus on write hits to keep that data consistent. In Dir_0B, the number of cycles used for directory accesses that cannot be overlapped with memory accesses is small relative to the total number of cycles. This result diminishes previous concerns that the directory itself could be a major performance bottleneck. In fact, the required directory bandwidth is only slightly higher than the bandwidth to memory. Techniques used to increase available memory bandwidth, such as distributing memory with the individual processors, can be applied to the directory as well. The fraction of cycles spent on invalidations is low, which implies that increasing this cost by a small factor will cause a relatively small increase in the total number of bus cycles used by Dir_0B. This result indicates that invalidating data in caches sequentially (rather than using a bus broadcast) may be viable without severely degrading performance. This case will be evaluated

[4] The Berkeley scheme, in addition, uses a different state for a dirty block that becomes shared to enable the cache to supply a block rather than memory. This optimization does not impact our performance metric in the pipelined bus.

The data in Tab'' 5 can be used to determine the system performance in a red-bus environment. The number of bus cycles consumed by a reference in the best scheme with a sophisticated bus is about 0.03 on average. In other words, a processor will use a bus cycle every 30 references, or a bus cycle every 15 instructions since on average each instruction in the traces makes one data reference. (We assume instruction misses do not cause bus transactions.) A 10-MIPS processor will therefore require a bus cycle every 1500ns, and a bus with a cycle time of 100ns will only yield a maximum performance of 15 effective processors. This limit is an optimistic upper bound because we have not included the bandwidth requirements of instruction misses, the effects of finite data caches, or the effects of bus contention.
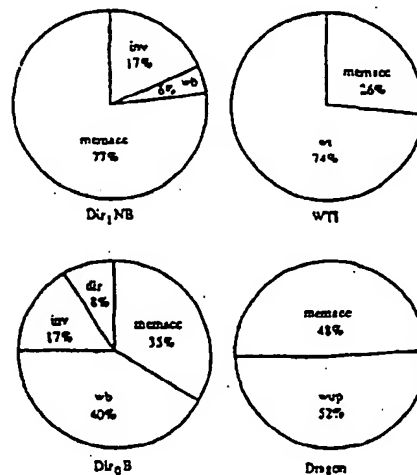
Figure 4: Bus cycle breakdown in the various schemes as a fraction of the total number of bus cycles used in the scheme. The code dir is directory access, inv is invalidate, wb is write-back, memacc is memory access, wt is write through, and wup is write update.

5.1 System Performance

Total system performance cannot be determined from the bus cycles metric alone. A better metric for this purpose is average memory access time as seen by each processor, but this metric requires many assumptions about the implementation of the memory hierarchy. Regardless of the memory system details, it is clear that the additional waiting time beyond the number of bus cycles for a reference as seen by the processor will be at least one bus cycle time. This additional "bus cycle" is used for initial cache access, propagation delay through the bus controller, and bus arbitration. Figure 5 shows the average number of bus cycles per bus transaction for each of

the schemes. Because the average Dragon c   is smaller than $Dir_0 B$, the performance of the Dragon sch...e will be more sensitive to changing that cost by a constant value. Consequently, for the metric of average memory access time as seen by the processor, we would expect Dragon to show less of an advantage than with the bus cycles metric.

Even using the bus cycles metric we can get an idea of the effect of adding a small constant number of bus cycles to the cost models. If q bus cycles are added to the cost of each bus transaction, the performance for Dragon is given by $0.0336 + 0.0206q$ and the performance for $Dir_0 B$ is given by $0.0491 + 0.0114q$ bus cycles per reference. For example, with $q = 1$ $Dir_0 B$ needs only 12% more bus cycles than Dragon, as compared with 46% in Figure 2.

5.2 Impact of Spin Locks on Cache Consistency Performance

Spin lock reads severely degrade the performance of the $Dir_1 NB$ scheme as measured by our bus cycles metric. The number of bus cycles in $Dir_1 NB$ is over a factor of six greater than the number used by $Dir_0 B$. As mentioned earlier one-third of the reads in POPS and THOR are due to spins on a lock. Because two processes often spin on the same lock, locks frequently bounce back and forth between two caches in the $Dir_1 NB$ scheme. To verify this phenomenon, we ran a set of experiments excluding all the tests on locks in the three traces. As expected $Dir_0 B$ gave the same performance as before, while the performance of $Dir_1 NB$ improved significantly (from 0.32 to 0.12 bus cycles per reference).

The impact of spin locking on the performance of the $Dir_1 NB$ scheme is also interesting in another light. Software cache consistency schemes that flush a critical section from the cache after each use will behave like the $Dir_1 NB$ scheme. For reasonable performance, these schemes must take special care in handling locks.

6 Directory Scheme Alternatives for Scalability

The need to perform full broadcasts limits the potential to scale a multiprocessor to a large number of processors. To obviate full broadcasts, pointers to all caches containing a block can be maintained in the directory ($Dir_n NB$ [9]). In this scheme, sequential invalidations are sent to each of the caches denoted by the pointers instead of using a full broadcast. We evaluated this scheme assuming that each invalidation consumes one bus cycle. The number of bus cycles per reference for a pipelined bus increases from 0.0491 in the full broadcast case ($Dir_0 B$) to 0.0499 in the sequential invalidate case ($Dir_n NB$). The performance degradation is small because often no more than one invalidation is necessary.[note]

Although the sequential invalidation scheme has comparable performance to the broadcast scheme, the directory size increases in proportion to the number of processors. The next scheme that we discuss capitalizes on the observation that a single invalidation request in the most common case. The directory maintains exactly one pointer and a broadcast bit

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[note] Note that our data was obtained from a machine with only four processors. We are trying to obtain traces for a much larger number of processes and hope to extend our results shortly.
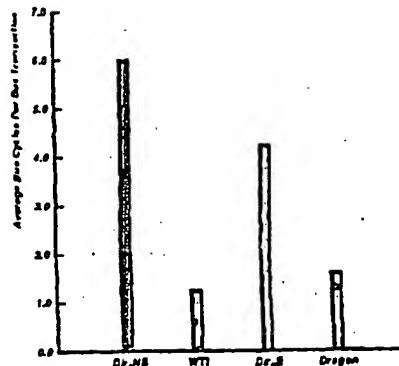
Figure 5: Average bus cycles per bus transaction in various schemes.

per block ($Dir_1 B$). If more than one cache has a block the broadcast bit is set. When the directory is queried, a single invalidation request is issued if the broadcast bit is clear: otherwise, the invalidation must be broadcast. While it is hard to quantize the exact effects of broadcasts, the following simple model can help indicate the performance of such a scheme. Suppose that a single invalidation takes one bus cycle as usual, and that a broadcast uses b cycles. With this simple model, this directory scheme requires $0.0483 + 0.0006b$ cycles per memory reference. This scheme can be extended to use i pointers ($i > 1$) and a broadcast bit ($Dir_i B$). The broadcast requirement can be eliminated if the number of allowed copies of a block is restricted to i as in the scheme denoted $Dir_i NB$. This scheme trades off a slightly increased miss rate for avoiding broadcasts altogether.

We can also use limited broadcasts if the caches where block copies exist are known. The number of bits in the main memory directory can be reduced by storing a simple code representing a set of caches, which is a superset of all caches with a copy of the block. For example, consider storing a word with d digits where each digit takes on one of three values: 0, 1, and both. If each digit in the word is either a 0 or a 1, then the word is the index to exactly one cache in the system. If any digit is coded both, then the word denotes caches whose indices may either be a 0 or a 1 in that digit, but match the rest of the word. If i digits are coded both, then 2^i caches are denoted. In like manner, we can code a set of caches that includes all block copies. Each digit can be coded in 2 bits, thus requiring $2log(n)$ bits in a system with n caches.

As the above examples show, a class of directory schemes exist that can trade off a small amount of performance for scalability and ease of implementation. An accurate evaluation of the tradeoffs will require traces from a much larger number of processors.

7 Conclusions

This paper shows that directory-based cache consistency schemes are an interesting approach for providing shared memory in a large-scale multiprocessor. The directory structure removes the major limitation of snoopy-cache schemes – the reliance on broadcasts – while providing similar efficiency in handling shared references. The bandwidth requirement to the directory, long considered a potential bottleneck, is shown to be not much more severe than the memory bandwidth need. The basic bandwidth limitation to the memory and the directory can be mitigated by distributing them on the processor boards. This technique allows the bandwidth to both the memory and the directory to scale with the number of processors.

We evaluated the performance of directory schemes in a small-scale multiprocessor environment using trace driven simulation. The performance of the directory protocols is reasonably competitive to the snoopy cache schemes. In addition the simulations show that most blocks that are written into are present in only a small number of other caches, which makes broadcast invalidates inefficient. This result suggests that a directory structure that stores with each block only a small number of pointers to caches containing the block is sufficient. If this data holds for large-scale multiprocessors, directories will provide an efficient method of implementing shared memory.

8 Acknowledgements

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SUPERFAST
BUS SUPPORTS
SOPHISTICATED
TRANSACTIONS

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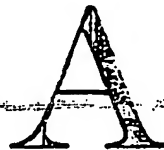
A new standard computer bus with the muscle to match the speed of the next generation of 32-bit systems is about to bow. Now being balloted by the IEEE, the proposed P896 Futurebus+ standard promises a maximum data-transfer rate of better than 50 million transfers/s, a 500 percent improvement over current 32-bit buses. What's more, Futurebus+ will be extendable to 256 bits.

The new bus will offer a lot to system designers. Its extremely high data-transfer rate makes it attractive for high-performance I/O operations, such as FDDI or high-resolution graphics. The fine task scheduling provided by the arbitration protocol is a requirement for real-time systems.

Also, its cache coherence, message passing, and split-transaction support allow the design of efficient multiprocessing systems. The standard has generated significant technological advances throughout its long development, starting 10 years ago as the original Futurebus. These include the creation of Backplane Transceiver Logic to boost bus performance, the development of high-performance asynchronous and source-synchronous data-transfer protocols, and the formulation of a unified theory of cache coherence. It is currently being examined with great interest by the user community as a step beyond the current generation of 32-bit TTL standards, such as the VMEbus and Multibus II. As it has the possibility of becoming a universal standard bus, it deserves close consideration by anyone designing a backplane-based system.

The performance of Futurebus+ can be expected to vary from system to system, depending largely on the data-transfer mode supported. The asynchronous, full-handshake mode (similar to that of the old Futurebus) uses burst transfers and can be expected to peak between 20 million and 25 million transfers/s. A new source-synchronous mode should operate at over 50 million transfers/s with the next generation of silicon support. Because Futurebus+ supports data-path widths of 32, 64, 128, and 256 bits, a raw data-transfer rate of 1.6 Gbytes/s is conceivable. Even at 32 bits, the 200-Mbyte/s source-transfer rate is five times the peak of VMEbus or Multibus II.

The original Futurebus standard was designed by a small group of dedicated visionaries without major corporate backing. The P896 committee, formed by the IEEE in 1979, wanted to create a single industry-standard 32-bit bus for multiprocessing systems. By the time the standard was approved by the IEEE in 1987, though, the industry-designed VME and Multibus II buses had already established a firm hold in the marketplace.

At the same time, the performance of these buses was being stretched to the limit by the new generation of cache-based reduced-instruction-set processors. So, rather than risk obsolescence, the manufacturers of existing 32-bit systems looked for a new platform upon which to develop applications. Futurebus was the only high-performance standard that could be revised and extended to meet the latest system requirements. That's because there is no large base of products already designed to the Future-
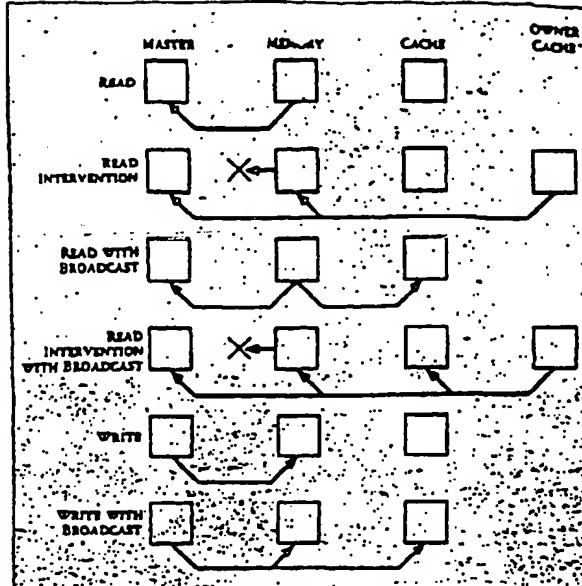
Figure 1. Futurebus+ provides transactions beyond the basic read and write to memory. Efficient multiprocessor cache-coherence protocols require that the bus support cache-induced intervention and broadcast.

bus standard, and its specs are still pliable.

The designers of the original Futurebus had already anticipated many of the extensions, such as faster data transfer and the caching protocol, and so the process of revising the standard went

THE FUTUREBUS
STANDARD HAS GENERATED
SIGNIFICANT TECHNOLOGICAL
ADVANCES THROUGHOUT ITS
LONG DEVELOPMENT

fairly quickly. A number of the changes, however, were incompatible with the 1987 version, and so the new P896 standard was renamed Futurebus+. Currently in ballot are documents covering the mechanical, electrical, arbitration, data-transfer, and bus-management layers of the specification, as well as the caching and message-passing protocols.

Expected to follow in short order are documents on the use of Futurebus+ in real-time and high-availability systems and those that describe special requirements for industrial and military operating environments. Standard bridges are also being specified to VMEbus and Multibus II.

Futurebus+ has been endorsed by vendors of existing 32-bit buses, including the VME International Trade Association and the Multibus Manufacturer's Group. It also has been selected by the U.S. Navy as one of the standards for future computer contracts.

The high speed of Futurebus+ is due to backplane transceiver logic, which was first produced by National Semiconductor in 1984. BTL was designed specifically to drive backplane transmission lines and provides the fastest possible bus interface in a CMOS or TTL environment. Its characteristics are the foundation upon which the Futurebus+ protocol rests.

BTL devices use open-collector drivers with an output capacitance of only 5 pF (possible because the drive transistor is isolated from the bus by a series Schottky diode). This allows the combined connector, trace, and package capacitance to

be limited to 10 pF for each slot, increasing the impedance of the backplane. ... also operates with a reduced signal swing of only 1 V and a precisely controlled switching threshold of 1.55 v. The result is that the backplane can be properly terminated at its fully loaded impedance, while allowing the drivers to cleanly switch the bus signals with only 50 mA of drive current.

With this interface technology, a bus designer can guarantee that a signal will cross the input thresholds of every receiver on the backplane on the incident edge of the propagating wavefront. A BTL bus never has to wait for reflections to settle before signals can be sampled. This allows Futurebus to implement much more efficient and high-performance data-transfer protocols than any TTL-based competitor.

☐ ARBITRATION

The Futurebus spec carefully works out an arbitration procedure designed to optimize the scheduling of requests from multiple modules and to prevent more than one module from trying to transfer data on the bus at the same time. Futurebus+ provides a large number of priority levels for accurate real-time task scheduling, as well as a fairness protocol that allows an even allocation of bus bandwidth to multiple modules. The arbitration takes place on its own independent set of lines in parallel with transfers on the data bus. The Futurebus arbitration mechanism provides a number of other facilities, including error detection and recovery, parking, bus-master identification, emergency messages, and a live insertion-and-withdrawal mechanism for board replacement in high-availability systems.

A real-time system requires that task priorities be assigned accurately. This guarantees the deadlines of periodic system tasks, decreases the response latency of the system to asynchronous events, and ensures that critical tasks will be completed even under heavy system loads. In order to achieve a high degree of task scheduling, Futurebus+ provides up to 8 bits (256 levels) of priority, which can be assigned dynamically to all system tasks.

In priority arbitration, the competing module with the highest priority always wins, and there is no limitation on the frequency of bus requests. Those modules that are subject to real-time constraint can be assigned priorities based on the maximum latencies they can tolerate. The only drawback is that mod-

FUTUREBUS WORKS OUT AN ARBITRATION PROCEDURE DESIGNED TO OPTIMIZE REQUEST SCHEDULING FROM MULTIPLE MODULES

ules with low priority may be completely shut out during periods of heavy bus usage. However, the dynamic allocation capability makes it possible to increase the priority of a long-waiting task.

In most time-sharing multiprocessing systems, though, processors need approximately equal access to the bus. If a task has been divided among a number of processors, the optimum performance results when all the subtasks are completed at roughly the same time. Futurebus+ provides a round-robin fairness protocol that can operate within each

priority level. Requests for the system at each level are serviced in the order of the competing module's unique ID field, typically based on slot position. The round-robin bit is set according to the ID of the most recent arbitration winner and serves to keep each requesting module's place in the circular queue. This scheme guarantees every module a fair slice of the overall bus bandwidth.

A Futurebus+ arbitration number consists of three fields, the 8-bit priority field, the 1-bit fairness field, and the 5-bit ID field. Because only 7 bits of the arbitration number can be applied to the bus during each competition, a module implementing full real-time priority assignment needs to win two arbitration cycles before gaining bus mastership. But in a typical multiprocessing system using only one or two priority levels, the most significant 7 bits of the priority field are 0s. Here, the arbitration can complete in a single cycle for maximum performance. Both types of systems are fully interoperable under Futurebus+.

Most events in a Futurebus+ system are signaled with a virtual interrupt mechanism, requiring direct access to

	CONNECTION	DATA TRANSFER	DISCONNECTION	
AS*				M
AK*				M & S
AI*				M & S
CM*				M
ST*				S
AD*	ADDRESS	DATA DATA		M & S
DS*				M
DK*				S
DI*				S

AS* = ADDRESS STROBE
AK* = ADDRESS ACKNOWLEDGE
AI* = ADDRESS ACKNOWLEDGE INVERSE
CM* = COMMAND
ST* = STATUS
AD* = ADDRESS/DATA
DS* = DATA STROBE
DK* = DATA ACKNOWLEDGE
DI* = DATA ACKNOWLEDGE INVERSE
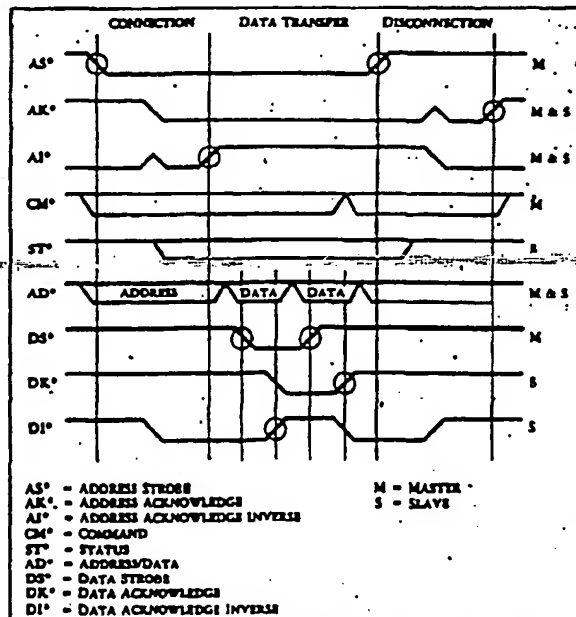
M = MASTER
S = SLAVE

Figure 2. Following the connection, or address phase, of the Futurebus+ transaction, the master transfers the card to its selected slave. Data releases the bus, possibly broadcasting additional information during disconnection.

physical interrupt signals in a Futurebus + backplane, so the arbitration protocol is used to fill this gap. Arbitration messages—special arbitration numbers that can be recognized by any module in the system—can be used to broadcast interrupts quickly, without first obtaining bus mastership or disturbing transfers in progress.

The arbitration protocol itself is based on an asynchronous three-wire handshake. This bus handshake controls the state machines within each module as they request the bus, perform the actual arbitration, check for errors and wait for the current bus master to complete its tenure, and transfer ownership of the bus. Arbitration performance depends on the modules participating in the protocol, but can typically be expected to range from 150 ns to 350 ns with existing technology.

□ DATA TRANSFER

Each transaction on Futurebus+ consists of a broadcast connection, or address transfer, followed by one of a variety of types of data transfer, and finally a broadcast disconnection. The connection phase is used to transmit addresses and commands from the master to the slaves, to return status to the master from the slaves, and for all participating modules to establish their data-transfer capabilities. Those modules that have been selected can participate in the data-transfer handshake, as can any caching modules that have chosen to "snarf" (induce data broadcast) or intervene. The disconnection phase is used to transfer information only during split transactions, when it provides the identity of the requester and the command of the response.

There are a number of transfer options that interact dynamically, providing a transaction set that supports applications ranging from the most basic to a multilevel-caching bus hierarchy. Transfers typically involve only the master and a single slave. However, because Futurebus+ was designed to allow multiple modules to maintain data coherence in shared-memory environments, the standard also provides support for broadcast and intervention (Figure 1).

Transactions also may be connected or split. The more typical is the connected transaction in which all data and status information are returned before that transaction are returned before the address handshake is complete. A split transaction, in contrast, typically consists of two transfers separated in time.

TABLE 1: COMMANDS

32- OR 64-BIT ADDRESSES
32-, 64-, 128-, OR 256-BIT DATA
READ AND WRITE

WORD AND PARTIAL-WORD TRANSFERS
UNLOCKED AND LOCKED TRANSFERS

CACHE-SHARING TRANSFER
CACHE-MODIFYING TRANSFER
CACHE-COPYBACK TRANSFER
CACHE INVALIDATE

CACHE-SHARING RESPONSE
CACHE-MODIFYING RESPONSE

SPLIT-TRANSACTION RESPONSE
REMOTE TRANSFER WITHOUT RESPONSE

PACKET-SIZE SELECTION
ATOMIC PRIMITIVE OPERATIONS

CACHE
COMMAND
BIT

SPLIT-FIRST
TRANSACTION
COMMANDS

TABLE 2: STATUS AND CAPABILITY LINES

STATUS

WAIT/END OF DATA
ERROR
INTERVENTION
CACHE SHARING
BROADCAST
SELECTED
BUSY
SYSTEM ERROR

CAPABILITY LINES

SPLIT-RESPONSE TRANSFER
COMPELLED OR PACKET TRANSFER
PACKET TRANSMIT SPEED

The first transfer, a request from the master to the slave, may include write data. The second transfer, generated by the slave, may include read data. Because both transfers are required, the split-transaction protocol is most useful during transfers across bus repeaters, where the data-access time can be much greater than the arbitration and address-transfer overhead.

The address/data path on Futurebus+ consists of 32 or 64 address/data lines on a single connector, with optional additional lines to support 128- or 256-bit data paths, and 8 user-definable tag bits. Each byte of the address/data highway is protected by a single odd parity bit. There are also an 8-bit command field (Table 1), protected by parity, plus

eight status lines and three capability lines (Table 2).

Futurebus+ provides a special set of commands to support the higher level cache coherence and split-transaction protocols, as shown in Table 1. A system that maintains the coherence of shared data among multiple modules requires that the master let other snooping caches know if it intends to keep a copy (share) of the addressed data or if it will write (modify) it. Likewise, the other caches must perform certain actions if they already have shared or modified copies of that data.

The Futurebus+ data-transfer protocol uses six synchronization lines. Three of these, the address-handshake lines, are used to establish and break a connection between a master and one or more slaves. The other three, the data-handshake lines, are used to transfer data or packets between the master and those slaves that have established the connection. In Futurebus+, information is usually transferred with every transition of these handshake lines.

Single-slave transactions involve only two modules and therefore have the most efficient data handshake (Figure 2). However, if another slave has an active request for the data being transferred—such as a cache with a pending request for that data—it can snarf the transaction and turn it into a broadcast. In either case, the directly accessed slave may not have the most recent copy of the data in a cache system. The cache that has modified the data internally must then intervene in the transaction, providing the updated data to the master and the selected (and any snarfing) slave.

Futurebus+ also has two distinct data-transfer modes: a fully handshaken, asynchronous compelled transfer and a high-performance, source-synchronous packet transfer.

The compelled data-transfer protocol uses an asynchronous handshake. Information is transferred from the master to the slave(s) between the transition of the data strobe and the release of one of the data-acknowledge lines. Information passes from the slave(s) to the master between that release and the next data-strobe transition. The transfer speed is controlled by all the participating parties, and it's limited by the round-trip handshake time—40 ns to 50 ns.

In the packet mode, the data handshake surrounds the transfer of an entire packet of data, and multiple packets can be transferred in a single transaction (Figure 3). Each packet is

transferred at a selected rate, synchronized to the source of the data. T transmit clock is embedded within the data on a bit-by-bit basis. Every packet consists of a sync bit, 8, 16, 32, or 64 NRZ data bits, and a parity bit that returns the data line to its original state. Because every bit is transmitted independently, there is no clock-skew timing penalty. The maximum transfer rate is probably limited by backplane physics at around 100 Mbits/s.

▫ CACHE COHERENCE

The Futurebus+ cache protocols allow this specialized memory to perform its three main functions automatically and completely transparent to the software. The first function is to convert a microprocessor's semirandom reads and writes into efficient burst transfers on the bus. The second is to provide the microprocessor with a fast local window into the system memory space. The third is to provide the basis for a multiprocessing architecture.

> **THE FUTUREBUS + CACHE**
>
> **PROTOCOLS ALLOW THE**
>
> **SPECIALIZED MEMORY TO**
>
> **PERFORM ITS THREE MAIN**
>
> **FUNCTIONS AUTOMATICALLY**

The original Futurebus cache task group developed the five-state MOESI cache-coherence model, the acronym coming from the five states—Modified, Owned, Exclusive, Shared and Invalid. MOESI was a superset of all previously known cache-coherence solutions, thereby allowing any combination of coherence protocols to coexist in the same backplane.

However, as the understanding of cache protocols improved, it became apparent that the complexity required to support the five-state MOESI model was not justified by the return in performance. So for Futurebus+, the group selected a four-state MESI copy-back protocol that can be generalized for caching over a hierarchy of buses using split transactions. Memory- and cache-agent pairs act as repeaters between processors on multiple buses accessing a single memory source.

In this cache-coherence protocol (Fig-
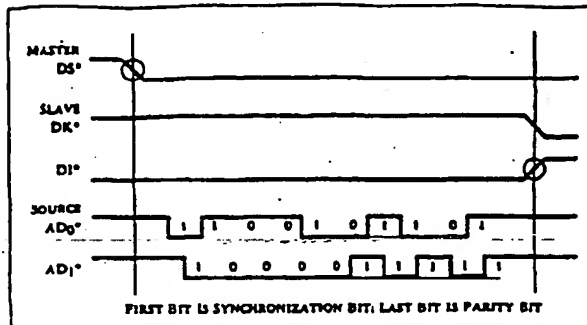
Figure 3. Packet-mode transfers allow a block of data to be transmitted at a predetermined source-synchronous clock rate. Since the clock is embedded in each data bit, ...

ure 4), every processor-cache line has associated with it one of four states: invalid (I); shared unmodified (SU); exclusive unmodified (EU); and exclusive modified (EM). In order for a processor to read data out of its cache, the data must first be valid—in the SU, EU, or EM state. If the data is invalid—in the I state—the cache must read the correct data from the bus. For a processor to write data, the cache must first ensure that no other cache has a copy of it; in other words, the cache must obtain an exclusive copy of the data—the EU or EM states. Once the processor has modified data in the cache—so that it is in the EM state—the cache must intervene or copy back to provide the system with the correct data.

A cache must modify its state information, or tags, in response to internal

processor and external-bus accesses, according to a set of rules described in the P896 standard. (Bus repeaters have a slightly different set of responsibilities, also described). An action by one cache affects every other cache in such a way that a consistent view of shared data is maintained. Futurebus+ provides the transaction set necessary to implement this shared-memory system efficiently. ▫

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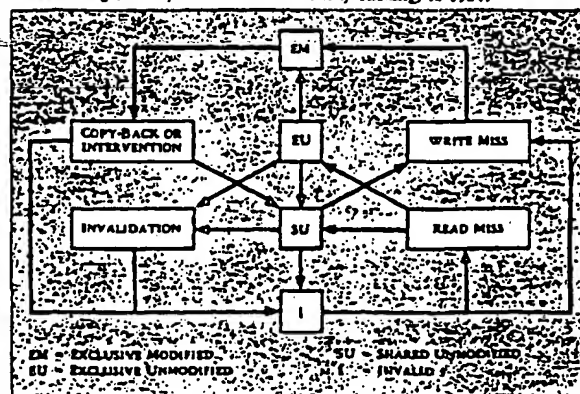
Figure 4. In the four-state cache-coherence model, a processor has private read permission if data is in the EM, EU, or SU states; it has private write permission in the EU and EM states; and it has responsibility to intervene in the EM state.

A 50-ns 16-Mb DRAM with a 10-ns Data Rate and On-Chip ECC

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Abstract—A high-speed 16-Mb DRAM chip with on-chip error-correcting code (ECC), which supports either 11/11 or 12/10 RAS/CAS addressing and operates on a 3.3- or 5-V power supply, is described. It can be packaged as a 2-Mb × 8, 4-Mb × 4, 8-Mb × 2, or 16-Mb × 1 DRAM, and is capable of operating in fast page mode, static column mode, or toggle mode. Speed and flexibility are achieved by a pipeline layout and on-chip SRAM's that buffer entire ECC words. The use of redundant word and bit lines in conjunction with the ECC produces a synergistic fault-tolerance effect.

I. INTRODUCTION

THE USE OF redundant circuits for increasing the manufacturing yield of integrated-circuit memory chips was proposed as early as 1969 by Chen [1] and, subsequently, by Arzubi [2] and Schuster [3]. The implementation of redundancy to large-scale integrated circuit manufacturing has been reported since 1979 [4]–[6]. More recently, the use of error-correcting codes (ECC's) has been investigated for the improvement of memory chip reliability [7]–[9]. The primary motivation for building such chips was their immunity to the so-called "soft errors" that are caused by alpha particles. The use of on-chip ECC circuits for overcoming the sensitivity to manufacturing defects and increasing the fabrication yield has been proposed by Yamada [10], Arzubi et al. [11], and Mazumder [12].

The combined use of redundant circuits and ECC is implemented on the 16-Mb chip described here. According to Stapper and Lee, this combination leads to a fault-tolerance synergism [13]. As a result, the chip's fault tolerance far exceeds the amount needed for current world-class integrated circuit manufacturing. Nevertheless, because of the fault tolerance, this chip can be fabricated in existing integrated circuit manufacturing facilities. It is made with a 0.5-μm CMOS process, using silicided polysilicon, two levels of metal, trench storage capacitors [14], and shallow trench isolation [15], [16].

A cursory description of this 16-Mb chip has been presented previously [17]. A more detailed discussion follows here. The chip's features and special functions are described in Section II. The chip layout is given in Section III, with separate subsections for array design, bit-line redundancy, word-line redundancy, ECC circuits, SRAM buffer, and off-chip drivers. The effect of the ECC and redundancy on yield and reliability is described in Section IV, while Section V deals with the packages for this chip.

II. CHIP FEATURES AND FUNCTIONS

The 16-Mb chip described in this paper is packaged in either 28- or 32-pin 400-mil SOJ modules. The 28-pin package meets the industry standard for 16-Mb chips. The 32-pin package has features that go beyond the standard industry functions. These features are activated with a $CAS + W$ before RAS and the appropriate address bits to select the desired operational mode or functions. The operational modes include fast-page, static-column, or toggle mode. Typical functions include page copy, page clear, 512-b parallel read–write test, soft-error scrub, partial write, and data selects. The external programming of these functions has no impact on the chip size, performance, or power. Output enable, internal row address counter, and multiplexed RAS and CAS addresses are standard features that require no programming.

The chip was designed for high speed. Its RAS access time is 50 ns, with a cycle time of 100 ns. In static-column mode the access/cycle time is 18/18 ns; in the fast-page mode the access/cycle time is 10/25 ns, and the toggle is 10/10 ns at 2.9 V and 85°C. The RAS access and fast-page access are shown in Figs. 1 and 2, respectively. Using a minor modification of the second-level-metal mask, the chip can be operated as a 3.3- or 5-V part.

The static column and fast page modes operate identical to the industry standards, but can also use optional block select inputs, sampled by CAS, to control writing or reading of their corresponding data input/outputs. The fast speed of these modes was accomplished by placement

Fig. 1. RAS access.

Fig. 2. Fast-page access.

of the static register, off-chip driver, and timing circuits next to the pads in the center of the chip. A special higher speed mode, toggle, is also provided. Toggle is a modified industry standard static column mode. The address input transitions start the cycle by selecting two bits behind each data input/output. The positive transition of toggle drives the first bit and the negative transition of toggle drives the second bit off the chip. While toggle is driving the second bit off the chip the address inputs can be changed to another random column address setting two new bits that are driven off chip by the next positive transition of toggle repeating the cycle. This provides a random column addressing on two bit boundaries with a continuous data transfer at a 10-ns rate. With the static register this allows the read operation to continue the length of the page even during the RAS precharge.

Using different wirebond or timing options, this chip can be used in a 2-Mb×8, 4-Mb×4, 8-Mb×2 or a 16-Mb ×1 organization, and 11/11 or 12/10 addressing. The 11/11 address mode facilitates the migration from 4-Mb DRAM's, and is useful for large memory systems that employ banks of memory, with most of the banks in the standby mode. The 12/10 address mode makes it possible to minimize power in unique applications. Both addressing modes use a CAS-before-RAS (CBR) of 2K addresses to maintain the lowest refresh power. The chip ECC provides an error scrub during the CBR refresh.

These features and other pertinent chip information are summarized in Table I.

TABLE I
16-Mb DRAM FEATURES

Cell Size	1.075 × 2.3 μm (4.15 μm²)
Cell Capacitance	100 fF
Bit Line Capacitance	332 fF
Chip Size	7.8 × 18.06 mm (140.86 mm²)
Configurations	×1, ×2, ×4, ×8
Performance	RAS 80/100 ns
	PP 10/30 ns
	SO 10/15 ns
	TOG 10/10 ns
Supply	3.3 × 3.3 V
	3.6 × 3.3 V
Productivity	B/L & WL Redundancy
	ECC (RRC/DED)
Features	Page-Copy
	Page-Clear
	× 512 Test Mode
	12/10 or 11/11 RAS/CAS Addressing
	CBR × 2K

III. CHIP ORGANIZATION AND LAYOUT

Fig. 3 is a photomicrograph of the 16-Mb chip. The actual chip dimensions are 7.8×18.06 mm. The photograph shows that the chip is divided into four quadrants. Each quadrant is a totally independent memory that can operate in either a 4-Mb×1 or 2-Mb×2 DRAM mode. The quadrants have their own individual bit redundancy and data steering, word redundancy system, error correcting circuitry, SRAM, and off-chip drivers (OCD's). These circuits are arranged in a "pipeline" order, providing the
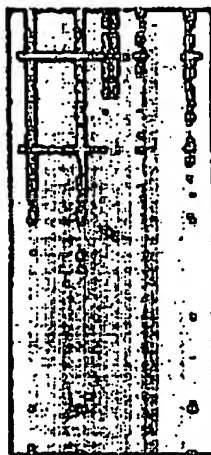
Fig. 3. Micrograph of a 16-MD chip.

Fig. 4. Quadrant layout.

most direct channel for the data flow. Furthermore, the bonding pads are located at the center of the chip. Therefore, signals travel less than half the chip length. This results in minimum *RC* wiring delays and provides the speed and performance for which this chip was designed.

The quadrants are divided into four array blocks (Fig. 4), each block containing 1024 word lines. Word decoding is done with NAND circuits to minimize area and optimize the performance trade-off between decoder speed and word-line length. Each word line contains 1112 b; 16 of the bits belong to the redundant bit lines, while the remainder belong to eight ECC words. An ECC word is 137 b long, consisting of 128 data bits and nine check bits. These ECC words are interwoven along the word lines, so that eight adjacent bits belong to eight different ECC words. In this way, clustered faults affecting adjacent memory cells are separated as individual cells of different ECC words.

Each block is further divided into two segments, each having their own interlocked timing generators. This results in minimum power consumption and maximum functionality. It also improves the chip reliability by isolating the faults, thus lowering the probability of multiple bit failures, and therefore minimizing the piece-part failure rate.

The two segments in a block are separated by sense amplifiers, local buffers, and a 1/16 decoder. The latter selects the sense-amplifier signals down to 139 b, representing one ECC word with two redundant bits, and puts this information in the local buffers. These local buffers,
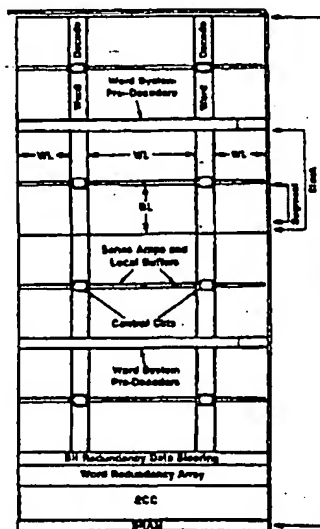
in turn, drive 139 second-level-metal buses known as pre-data lines (PDL's). A functional block diagram of the quadrant arrangement is shown in Fig. 5. Note that detail is shown for only one of the array blocks.

The 139 PDL's run in the same direction as the first-level-metal bit lines. To prevent capacitive coupling to any particular single bit line, the PDL's zigzag across the array at three degree angles, reducing the capacitive loading by one sixteenth while only incrementally increasing the PDL length. The zigzagged PDL's also present an equal load to all the bit lines independent of mask misalignment.

The PDL's send the data to the data-steering circuits for the bit redundancy, where the two redundant bits can be used in an any-for-any replacement of faulty bits. If, however, the data came from a defective word line, the entire 137-b word can be replaced with information stored in a separate DRAM array containing 24 redundant word lines, each 1096 b long. Data from either the DRAM or the word redundancy array are passed on to the ECC circuits, where any single failing bit is corrected and multiple failing bits are detected. The output from the ECC circuits is sent to a SRAM register. The SRAM is decoded by the low-order CAS addresses, and the SRAM data are driven via the off-chip drivers to the bonding pads. Since the ECC circuits, SRAM, off-chip drivers and pads are located next to each other, this architecture
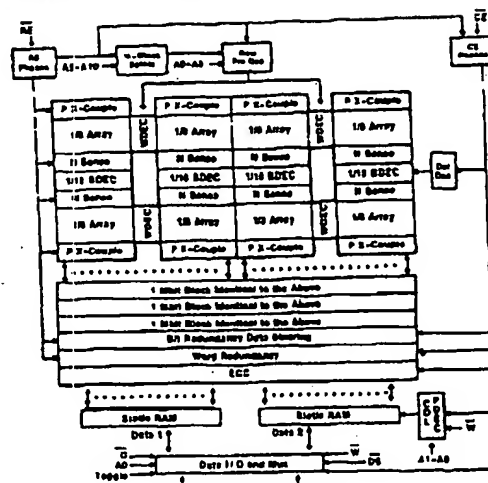
Fig. 5. Quadrant block diagram.
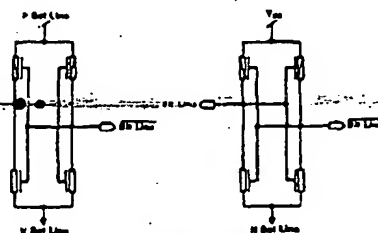
Fig. 6. Sense-amplifier circuits.

provides for an efficient layout with a minimum ECC logic delay of 5 ns for the first bit accessed, and no delay for subsequent bits accessed.

A. Array Design

The chip uses a p-array that has been described previously [14]. The array bit lines and word lines are both biased at $V_{dd} = 3.3$ V during standby. This provides protection against defects that could cause short circuits between word and bit lines. During standby such defects cause no additional current drain. Furthermore, when active, the bit line follows the word-line voltage, thus causing a bit-line failure without current flow. This makes

it possible to use redundancy or the ECC to replace or correct the bit lines affected by these defects.

This biasing scheme ($V_{dd} = 3.3$ V) can provide the lowest power dissipation in the array during active cycles when the chip is operating in the 3.3-V mode. If, while operating in this mode, an alternative precharge bias other than V_{dd} had been used, and if all power dissipation in the array and support circuits was taken into account, the total power dissipation could be equal to or greater than the power dissipated when the bit lines are biased at V_{dd}.

With low bit-line precharge biases, the drive of the sense amplifiers is reduced. This extends the time to amplify the signal and, during array setting, can increase

current surges. It is well known that the pulse used to set a sense-amplifier node can be adjusted to provide current only in the "on-side" device at a sacrifice in speed, and that there is a speed increase when there is some conduction in the "off-side" of the latch [18]-[22]. Increasing the off-side conduction current too much reduces the amplifier's sensitivity and increases current surges without any further performance improvements. This becomes of importance in a 3.3-V design with the bit lines precharged at $V_{dd}/2$. In that case, the gate drive is so low that the time required to amplify the bit-line signal is excessive. Therefore, it is not viable at this low voltage level to skew the p- and n-set phase lines in the circuit shown in Fig. 6. Furthermore, during setting of the amplifier, with both on-side and some off-side conduction in the latch, a very large crossover current can be present when charging or discharging the bit-line capacitance. This crossover current flows from p-set to n-set, and is comparable to a short-circuit current from V_{dd} to ground in a switching inverter.

Using p-channel load devices and n-channel set devices, and maintaining off-side conduction at the level of maximum performance with minimum off-side voltage droop, the power dissipated is minimized. The array power dissipation is primarily the CV^2/T dissipation resulting from charging/discharging the bit lines and the n-set line. When the bit lines are biased at a voltage lower than V_{dd}, the crossover current defined above is not the only cause for power loss contributing to the array power dissipation. There are many other causes. One of these is the voltage regulator required to prevent the bit lines from drifting during a long restore, and to hold the bit lines at a voltage other than V_{dd} or ground. Also, driving of the p-set line capacitance dissipates power. Finally, the size and the number of devices required for bit-line equalization increases. To maintain the same bit-line equalization performance as with the full V_{dd} bias, the device sizes must be increased to compensate for the lack of gate drive and more devices are required to control additional nodes. The capacitive load of the phase to drive the equalization can easily increase by a factor of 8. When all such causes for power dissipations are taken into account, their sum can be equal to or greater than the power required for moving the bit-line potential with a full V_{dd} voltage swing.

All unselected arrays in this 16-Mb chip design are kept connected to V_{dd}. This results in large on-chip decoupling of the power buses, thus providing a low-noise array and support circuit environment. This is difficult, if not impossible, to achieve if the bit lines are not restored to supply levels.

The signal development speed of the p-array is enhanced by restoring the bit lines to V_{dd}, because signal development starts as soon as the word line and reference word line reach a voltage equal to V_t. This also contributes to the speed attained by this chip. During the write-back of the signal into the storage-cell capacitor, the word line is "mini-boosted" to enhance the signal stored in minimum time since the cell device operates in a
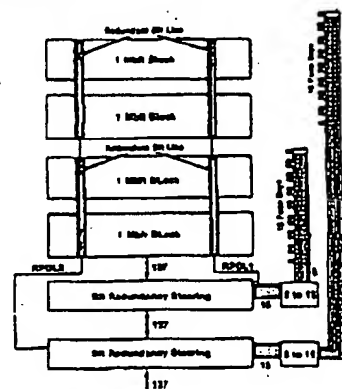
Fig. 7. Bit-redundancy system.

source-follower mode. During the read a voltage boost is not required since the cell device is operating in a grounded-source mode with large overdrive. For an n array, the equivalence is achieved by biasing the word lines and bit lines to ground, and using n-channel load devices and p-channel cross-coupled pairs for sensing.

B. Bit Redundancy and Data Steering

Defective bit lines are replaced independently for two array blocks of each quadrant. Since there are 16 redundant bit lines per block, this results effectively in 32 redundant bit lines per quadrant. A block diagram of the redundancy system is shown in Fig. 7. Note that the groups of redundant bit lines are physically separated at different places in the array. This minimizes the possibility of clustered defects affecting the two redundant lines associated with any specific ECC word. As shown in Fig. 7, the redundant PDL's (indicated as RPDL1 and RPDL2) are therefore located in different parts of the array.

The addresses of faulty bit lines are stored in 32 fuse banks, or fuse bays. The identity of the fuse bay indicates the address of the bit line that needs to be replaced. The eight fuses in each fuse bay contain the information for replacing the PDL's with the data from the defective bit lines. This approach not only saves fuses, but has a number of other advantages. The information from the fuse bays is always available to the redundancy steering circuits, whether it is needed or not. Furthermore, since the fuse information is stored in registers consisting of simple latch circuits, it is possible to enter this information into those latches externally without blowing the fuses. This is done by using one of the programming codes for selecting the optional features of this chip. This
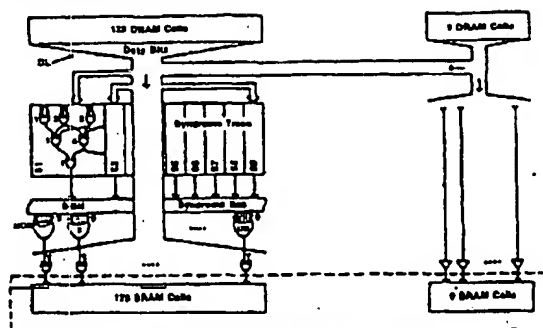
Fig. 8. Read operation with ECC circuits.

procedure is referred to as "soft blow," since the fuses do not have to be blown to set the redundancy.

C. Word Redundancy

Word-line redundancy is implemented by replacing defective word lines in the main array with ones in an additional (redundant) array. Similar to the bit-line redundancy, the addresses of defective word lines are programmed into the chip by either blowing fuses with a laser, or by using the soft-blow technique with one of the programs for optional features. By either method, when a defective word line is accessed, the word redundancy system cuts off the data from the main array and replaces it with data from a word line in the redundant array.

The word redundancy array (24 word lines by 1096 bit lines) operates independently of the main DRAM array. It incorporates a twin cell that stores both true and complement data. The small size of this array makes the added area of the twin cell small compared to the support circuitry. A further advantage of the small array size is a high transfer ratio resulting from the short bit lines. Since both the true and complement data are stored in a twin cell, this memory requires no reference cells. The combination of twin cells and short bit lines results in a signal that is an order of magnitude larger than the signal of the ordinary cell/reference cell configurations. As a result, the word redundancy array is less prone to failure and results in higher yields per word line.

The defective word-line addresses are also stored in fuse bays. Each fuse bay is dedicated to a word line in the redundant array. The data in the fuse bay determine whether an addressed word line should be replaced by comparing the data on the address bus with the address data stored in the bay. If the addresses match, the bay's word line in the redundant array is used to replace the word line selected in the main array. Any fuse bay can be programmed to replace any of the 4096 word lines in a quadrant.

D. Error-Correcting Circuitry

The use of ECC circuits on a chip leads to a delicate trade-off between performance, chip size, and yield or reliability enhancement. An odd-weight Hamming code with double-error detect/single-error correct (DED/SEC) is used because it provides a lower cost than codes like the horizontal–vertical (HV) parity ECC system [23]. An optimum code was found by using 128 data bits and nine check bits [24]. These check bits indicate the correct logic states of the data bits. The ECC logic tests the data bits, using the check bits, to generate syndrome bits. The syndrome bits indicate which bits in the ECC word are faulty. The ECC logic uses this information to correct the faulty bits.

All of the read or write cycles of this chip begin with a "fetch" operation, followed by a "write-back" operation. During the fetch operation, the ECC circuits receive inputs from either the memory cells in the DRAM array, or from the word redundancy array. After passing through the ECC circuits, the correct ECC word is stored in the SRAM, which includes the nine check bits and the 128 data bits referred to as a "page." Bits are selected from this page and sent to input/output (I/O) bonding pads. A flow diagram of this operation is shown in Fig. 8. During the write-back, data are transferred from the SRAM through the ECC circuits to the DRAM array or word redundancy array. A flowchart of this operation is shown in Fig. 9.

The ECC circuits were designed using a differential cascode voltage switch (DCVS) logic tree [25]. An example of four-input XOR circuit of this type is shown in Fig. 10. These circuits are small and fast, resulting in a typical logic delay of 5 ns through the ECC tree. Because of the error correction, the total increase in chip area is 15 mm² (11% of the chip area), including all cells, sense amplifiers, logic, and wiring associated with the ECC.

These DCVS logic circuits also have a unique failure mode that can be used to great advantage. The outputs of
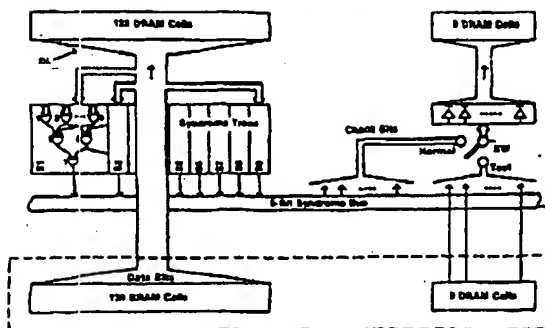
Fig. 9.   Write operation with ECC circuits.
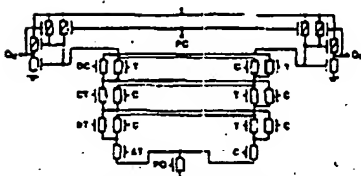
Fig. 10.   DCVS logic circuits.

a logic circuit are both zero until set. When the circuit is set, only one of the outputs will be a one. Faults in the logic will therefore create either a double-zero or double-one output. When these matching output pairs propagate through the logic, they are easily detected. By using nine observable test points, it is possible to get 100% test coverage of the ECC circuits with only 37 test vectors.

E. SRAM

The output of the ECC circuits is placed in an SRAM register. Since the register is located next to the off-chip drivers and I/O pads, this results in high data rates. The SRAM register also allows a $\times 512$ test mode that can do complete pattern sensitivity testing, with any combination of writes and reads at normal chip cycle time. As shown on Fig. 11, the register is loaded in parallel with the data provided to the receiver during a write cycle. The register bits are then stored into the unique cell locations every 8 b apart along the word line. During read, the bits put in the register are compared with each other. If all the bits are identical, the chip output will be a one, otherwise the output is zero. The chip is initially tested to repair any faults with word-line and bit-line redundancy. Then, complete pattern testing can be done in a test-characterization mode with the ECC circuits turned off for verifica-

tion of all 137 b. In a customer environment, the testing can be done with ECC turned on, thus verifying the integrity of the 128 data bits. The test can be simultaneously performed in all four quadrants, thus allowing the verification of 512 b at the same time. This provides greatly improved module, card, and system memory test time.

F. Off-Chip Drivers

A rate-controlled off-chip driver circuit was developed to support the chip's fast data rate. This circuit suppresses the current surges usually associated with off-chip drivers, especially on chips operating in the $\times 8$ mode. A circuit diagram is shown in Fig. 12. The output rise or fall time of the circuit is continuously sampled through an RC bias network, which biases a device network at the verge of conduction. This device network drives the second output device with an analog gate control. The first output device sets the fastest rate for a minimum load under optimum conditions. The drive on the gate of the second device varies as a function of the output load. It therefore maintains a constant rate of voltage change regardless of power supply, output load, process, or temperature. As a result the power supply noise for internal circuit operation is minimized, and the chip provides well-controlled pulses and signals to the external memory wiring and circuitry on memory cards.

This driver circuit controls the output rise/fall time to 1 V/ns.

IV.   Yield and Reliability Enhancement with ECC

The error-correcting circuits in the 16-Mb chip can be very effective in correcting single cell failures. However, any additional faults in an ECC word must be fixed with redundancy or the chip will fail. In order to optimize the

Fig. 11. Test-mode functional block diagram.

Fig. 12. Rate-controlled off-chip driver.

Fig. 13. Yield curves for ECC and bit-line redundancy.

fault tolerance of a chip with error correction, it is necessary to replace the ECC words that contain more than one faulty cell. The first step in achieving this is the use of bit-line redundancy. This approach is optimized by the chip layout because, effectively, the chip consists of 64 data blocks which are referred to as "books." Each book contains 2048 ECC words and two redundant bit lines. The redundant bit lines contain 2048 b each, making it possible to replace any defective bit in a book. Computer simulations and theoretical calculations show that the fault tolerance dramatically increases by this use of redundant bit lines and ECC. The resulting yield as a function of the average number of failing single cells per chip is shown in Fig. 13.

It is important to explain the curves in Fig. 13. Without the use of the ECC circuits, using redundant bit lines only, an average of 28 randomly failing single cells per chip would result in an expected yield of 50% for this
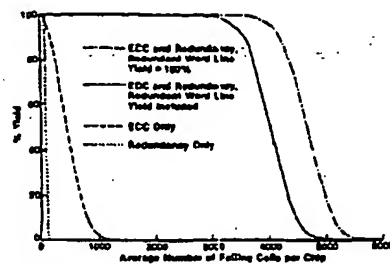
Fig. 14. Yield curves for ECC and word-line redundancy.
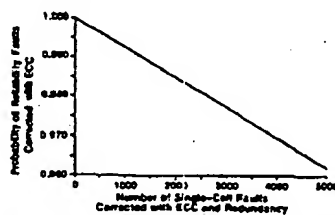
Fig. 15. Effectiveness of reliability improvement with ECC in the presence of hard fails.

chip. Using the ECC circuits only, and no bit-line redundancy results in a 50% yield for and average of 428 random single-cell failures per chip. Combined use of the redundancy and ECC produces a 50% yield at an average of 2725 randomly failing single cells per chip. This effect is, therefore, synergistic.

It was determined analytically how the 50% yield point depends on the number of redundant bit lines per book [13]. This point can be moved out sharply as a function of the number of redundant bit lines. Nevertheless, for the 16-Mb chip described here, this number was kept to two redundant bit lines because even better fault tolerance is achieved by the use of redundant word lines.

As mentioned earlier in this paper, there are 24 redundant word lines in a quadrant. A redundant word line contains eight ECC words. Therefore, if one or more of these words contain multiple defects, they can be replaced by a single redundant word line. This capability makes word-line redundancy more effective than the bit-line redundancy in enhancing the fault tolerance. The chip yields resulting from the use of word-line redundancy and ECC are shown in Fig. 14. The chip yields are affected by the yield of the redundant word lines. If the yield of the redundant word lines is assumed to be the same as that of the regular word lines, the 50% yield point occurs at an average of 4016 random single-cell failures.

Fig. 16. SOJ modules.

Since the redundant word lines use as twin-cell technology, they are less sensitive to defects than the regular word lines. Assuming 100% yield for these redundant lines results in a 50% yield point at an average of 4661 random single cell failures per chip.

The analytical solution for the yield resulting from the combined use of word- and bit-line redundancy with ECC has not yet been found. Simulations, however, have shown that the results can exceed the rightmost curve in Fig. 14. The capability of this fault tolerance technique is therefore truly awesome, and exceeds the current fault tolerance needs for world-class memory chip manufacturers.

The major application of ECC circuits on memory chips has been for the increase in reliability. However, even when the ECC circuits are used to fix "hard" manufacturing defects, the reliability improvement capability of those circuits is barely affected. Fig. 15 illustrates the effectiveness of ECC circuits in correcting reliability failures as a function of the number of hard random single cell failures originally on the chip. Note that, if there were 5000 hard random fails on a chip corrected with the ECC circuits, an additional single cell reliability failure would still have a 96% chance of being corrected with the ECC.

V. PACKAGES

The chip can be packaged in a 28/24-pin SOJ module and meet the industry standards. However, this limits its actual functionality. When packaged in a unique function 32-pin SOJ module, 400 mils wide and 825 mils long, it is capable of operating with the special functions and the extended features discussed earlier. This package has dual in-line leads at a 50-mil lead pitch. The most common operation of this module is with a 4-Mb × 4 organization and toggle mode. The pin-out for these modules is shown in Fig. 16. Also shown is a module for a 2-Mb × 8 organization.

tended to all others who helped make this chip a reality, in particular the many people involved in the device development, process development, mask build, test development, test characterization, software analysis, and checking.

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An Experimental 16-Mbit CMOS DRAM Chip with a 100-MHz Serial READ/WRITE Mode

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Abstract —A 5-V 4M word×4-bit dynamic RAM with a 100-MHz serial READ/WRITE mode has been designed and fabricated using 0.7-μm triple-tub CMOS technology. The RAM utilizes a newly developed STT (STacked Trench capacitor) cell which achieved 37 fF in a small cell size of 1.7×2.6 μm². The STD (Sidewall Transistor with Double doped drain) structure has been introduced for PMOSFET's to realize high-speed operation, and in order to ensure the MOSFET reliability the 5-V external supply voltage is converted to a 4-V internal supply voltage by an on-chip voltage converter circuit.

A new on-chip interleaved circuit and double-input-buffer scheme have been introduced to realize a high-speed serial READ/WRITE operation. Using an external 5-V power supply, the RAM achieved a 100-MHz serial access cycle, and the *RAS* access time is 70 ns. The typical active current is 120 mA at a 190-ns cycle time.

I. INTRODUCTION

AN EXPERIMENTAL 16-Mbit CMOS DRAM with stacked trench structure cells will be described in this paper. In order to realize 16-Mbit DRAM's, a large number of design constraints must be overcome.

The purposes of this 16-Mbit DRAM chip are to examine the feasibility of the STacked Trench-capacitor-(STT) cell, the Sidewall Transistor with Double doped drain (STD) structure, the on-chip interleave circuit, and the double-input-buffer scheme.

In the following section, the 16-Mbit DRAM memory cell design, using a new stacked trench capacitor in an optimized cell-p-well, is described. In Section III a MOSFET design that allows high-speed operation and ensures reliability is described. In Section IV array design and layout design are described. In Section V an on-chip interleaved circuit and a double-input-buffer scheme are described. Section VI summarizes the performance and other characteristics of the chip.

II. MEMORY CELL DESIGN

In developing large-scale integrated MOS memory, such as 16-Mbit DRAM's, the most important issue is to achieve large cell capacitance in a small cell area. Miniaturization of the conventional planar cell seems to reach the limit of fulfilling this requirement in 4-Mbit DRAM's and beyond. Therefore, three-dimensional DRAM cells, such as a trench capacitor cell, a stacked capacitor cell, and a buried stacked capacitor cell, have been intensively studied [1]–[4]. However, these cells have disadvantages when applied to 16-Mbit DRAM's. A stacked capacitor cell stores charge in the polysilicon node which is stacked on the cell area, and the cell capacitor can overlap the isolation oxide. Therefore, the cell capacitor area of the stacked capacitor cell is larger than that of the planar cell and it is one of the most promising cells for 4-Mbit DRAM's. However, it is difficult for the stacked capacitor cell to achieve large enough cell capacitance in further miniaturized cells, for 16-Mbit DRAM's and beyond, without forming and utilizing vertical surface in the cell. From this point of view, the buried stacked capacitor cell is a good candidate for 16-Mbit DRAM's. Fig. 1 shows a typical buried stacked capacitor cell, which is composed of a stacked capacitor buried in an isolated trench and a switching transistor. Therefore, the capacitor area can be enlarged sufficiently by deepening the trench without any cell size penalty. However, the buried stacked capacitor cell has an *intracell* current leakage problem. A gate-controlled diode structure is formed at the source junction of the switching transistor, as shown in Fig. 1. This diode structure causes a large current leakage at the storage node. Fig. 2 shows the junction leakage current characteristics of the cell. The junction leakage current shows a large peak around $V_s = 0$ V where the damaged trench sidewall is depleted. The memory cell data are strongly affected by this leakage current due to generation centers, which are introduced by reactive ion etching of the trench, in the depletion region.
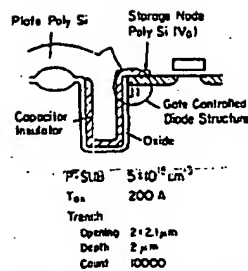
Fig. 1. Junction leakage characteristics of the buried stacked capacitor cell. A gate-controlled diode structure is formed at the source junction of the switching transistor.
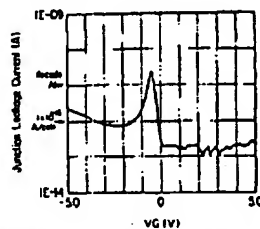
Fig. 2. Junction leakage characteristics of the buried stacked capacitor cell.

Fig. 3. Schematic cross-sectional view of the STT cell

Fig. 4. Fabrication process of the STT cell.

Fig. 5. Cross section SEM photograph of the STT cell from the fabricated 16-Mbit DRAM.

A trench cell is relatively easy to manufacture and to introduce into the DRAM process sequence. However, a trench capacitor cell directly uses the etched trench sidewall as a capacitor electrode. Therefore, the cell suffers from capacitor reliability problems [4]–[6]. In miniaturizing the cell area, intercell punchthrough leakage arises.

In order to overcome these problems, the STT cell has been developed and utilized in the 16-Mbit DRAM [7], [8]. Fig. 3 shows a cross-sectional view of the STT cell. The cell is constructed with a polysilicon-to-polysilicon capacitor in a trench and sidewall diffusion layer, into which impurities are diffused from the first-level polysilicon. Consequently, highly reliable low intracell leakage current has been realized. Moreover, using the sidewall process for the first-level polysilicon in the STT structure, the effective trench opening can be made smaller than that of the trench cell, which is limited by the lithography process. Therefore intercell punchthrough has been suppressed compared with the trench capacitor cell. Oxide-nitride-oxide dielectrics are used for the capacitor insulator. The third polysilicon layer is used for the switching transistor, and the bit line is made of Mo-Si polycide. Fig. 4 shows the fabrication process of the STT cell and Fig. 5 shows an SEM cross-sectional view of the cell. The cell measures $1.7 \times 3.6 \ \mu m^2$. The cell achieved a large cell capacitance of 37 fF using a 4-μm-deep trench with an 0.8-μm opening. The intercell leakage current has been decreased successfully by miniaturizing the sidewall diffusion length, less than 0.1 μm, and optimizing the depth and the concentration of the p-well.

III. MOSFET DESIGN

Use was made of 0.7-μm CMOS technology for the peripheral circuit to achieve high-speed, low-power operation. Fig. 6 shows a cross-sectional view of 0.7-μm CMOS

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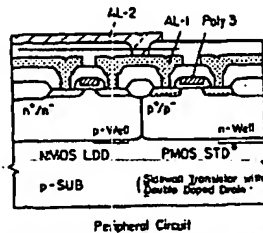
Fig. 6. Cross-sectional view of 0.7-μm CMOS technology for the peripheral circuit.
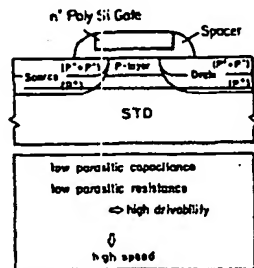
Fig. 7. Schematic cross-sectional view of the STD structure.
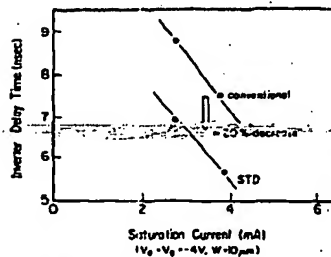
Fig. 8. Propagation delay time of conventional CMOS and STD CMOS inverters.

Fig. 9. Equivalent circuit of the on-chip voltage converter.
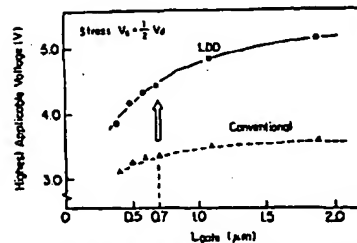
Fig. 10. Highest applicable voltage for conventional and LDD NMOS. Highest applicable voltage is defined as voltage at which transconductance degradation rate is less than 10 percent during 10 years of stress under the condition of 0.1-percent duty ratio.

for the peripheral circuit. Since the memory cell is formed in a deep high-concentration p-well optimized for the STT structure, the peripheral p-well is optimized for peripheral CMOS and the chip utilizes the triple-tub technology. To realize high-speed operation the STD was used for PMOSFET's [9]. Fig. 7 shows a schematic cross-sectional view of the STD structure. This structure has a source/drain p⁻ region surrounded by an optimized p⁺

region, and it minimizes the gate–drain overlap capacitance without series resistance penalty. Fig. 8 compares the propagation delay time of conventional CMOS and STD CMOS inverters. A 20 percent higher speed has been obtained by the STD structure [8]. In order to realize high reliability, an internal voltage converter is implemented on the chip. Fig. 9 shows the newly developed on-chip voltage converter. It consists of an optimized two-stage internal voltage sense circuit and a PMOS load transistor. The most important constraint here is the design of the internal voltage supply. Utilizing a LDD structure for NMOSFET's, a 4.0-V internal supply voltage can be used while maintaining high reliability and high performance, as shown in Fig. 10 [9].

IV. ARRAY DESIGN

In order to realize high-speed, low-power operation, two new circuit technologies, a new chip layout technique and the partial activation scheme, have been introduced for the array design.

The new chip layout is shown in Fig. 11. The wiring delay cannot be ignored in the design of a high-speed
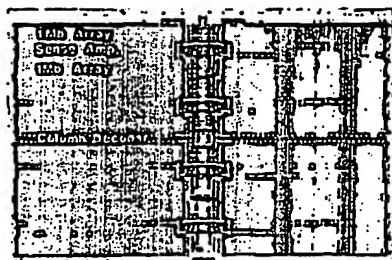
Fig. 11. 16-Mbit CMOS DRAM chip photomicrograph.

Fig. 12. Block diagram of the interleaved circuit implemented in 16-Mbit DRAM.

Fig. 13. Timing diagram of the serial READ cycle.

16-Mbit DRAM. To minimize the wiring delay without sacrificing chip size, the peripheral circuit and decoders are placed at the center of the chip, and a double-level aluminum process is introduced. In large-scale memory, the power dissipated in the memory cell arrays increases significantly. In order to reduce the active current, a one-fourth partial activation scheme [10] has been adopted.

Together with the one-fourth partial activation scheme, a shared sense amplifier has been introduced to reduce the chip area.

V. A 100-MHz SERIAL READ/WRITE MODE

In addition to normal RAM functions, this RAM has a 100-MHz serial READ/WRITE mode. Using this mode data from 1×4 to $2K \times 4$ bit can be serially accessed. This function will find wide memory applications in various image processing systems, especially in the high-definition TV systems being developed. In order to realize real-time image processing of the high-definition TV, the RAM has to transfer 2-kbit data serially with a signal rate of more than 74 MHz. Current RAM's with the nibble mode [12] or the dual-port configuration [13], [14] do not meet these requirements. The data rates of these RAM's are below 50 MHz, not fast enough for high-definition TV applications.

An on-chip interleaved circuit which makes it possible to read or write serial 2-kbit data continuously without extra chip area solves this problem. Fig. 12 shows a block diagram of the interleaved circuit implemented in this 16-Mbit DRAM. The cell arrays are divided into four blocks, with each block having an input port and an output port. Each block is composed of two 2-Mbit cell arrays (A and B banks) activated by clocks ϕ_a and ϕ_b. These banks are selected alternatively. When clock ϕ_a is activated, 4 bits of data are serially read out to the data-out port from shift register A, and simultaneously 4 bits of data from bank B are transferred to shift register B. In the next cycle, when clock ϕ_b is activated, the 4 bits of data already transferred in the previous cycle to shift register B, can be read out to the data-out port serially from shift register B, and simultaneously, the 4 bits of data from bank A are transferred to shift register A. This sequence is
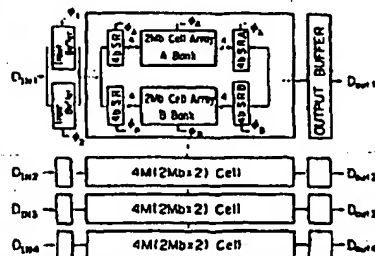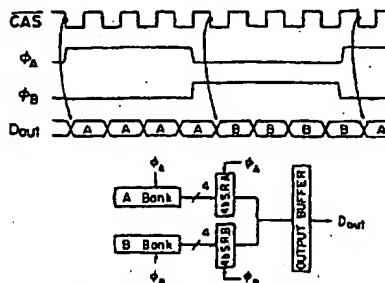
illustrated in Fig. 13. Using the column address counter, up to 2 kbit of serial data can be read out continuously without spending any idle time.

In order to attain a 100-MHz serial WRITE cycle, the input circuitry should be improved. A double-input-buffer scheme has recently been introduced in this chip. Each input port of present DRAM's has only one input buffer. This buffer is used for two purposes: one is to sense and latch the input data; the other is to transfer the data to the RAM. The single buffer cannot execute these two operations concurrently. Thus, the input data rate is restricted. This RAM has two input buffers per input port. While one input buffer receives the input data, the other can transfer previous data by using complementary clocks ϕ_1 and ϕ_1, as illustrated in Figs. 13 and 14. Using the double-input-buffer scheme, the input data rate is doubled and a 100-MHz serial WRITE cycle is obtained.

VI. CHIP CHARACTERISTICS

A microphotograph of the die, which measures 17.5×12.0 mm^2, is shown in Fig. 11. The RAM consists of 16 sets of 1-Mbit blocks. The peripheral circuit and row/col-

Fig. 14. Timing diagram of the serial WRITE cycle.

Fig. 15. Observed operating waveforms of the random access mode.

Fig. 16. Measured internal waveforms by an EB tester during the random access mode.

Fig. 17. Typical schmoo plot of external V_{cc} versus RAS access time.

Fig. 18. Retention time of 16-Mbit CMOS DRAM. The retention time is defined as the time when 50 percent of the total bits fail.

umn decoders are placed at the center of the chip to minimize the wiring delay.

Fig. 15 shows the operating waveforms of the random access mode. Typical RAS access times as small as 70 ns have been obtained. Fig. 16 shows the internal waveforms measured by an EB tester. The RAM is found to operate stably, as predicted by SPICE simulation [15]. A typical schmoo plot of external V_{cc} versus RAS access time is shown in Fig. 17. This RAM shows the wide operational margins for the external supply voltage.

The active current is typically as small as 120 mA at 190-ns cycle time.

The retention time, defined as the time when 50 percent of the total bits fail [16], of the RAM is shown in Fig. 18. The retention time of the chip using a trench cell is also shown as a reference. The retention time is about 1 s at 85°C, which is as long as that of a trench cell. The activation energy of the retention time is calculated to be 0.55 eV. This value is very close to half of the Si-bandgap energy, which shows that the leakage phenomenon in the STT cell is due to the recombination current at the junction. From these results, the STT cell seems to be quite promising for 16-Mbit DRAM's.

The observed operating waveforms of the serial READ/WRITE mode are shown in Fig. 19. A 10-ns serial cycle time has been achieved under a 5-V external supply voltage. The measured 100-MHz serial data rate is fast enough for a high-definition TV system. Table I summarizes the main features of the experimental 16-Mbit DRAM's.

VII. CONCLUSION

A high-performance 16-Mbit CMOS DRAM has been successfully fabricated. The chip utilizes the highly reliable and manufacturable STT cell and the high-speed STD structure. The circuit design used in this chip features new

├── 10ns
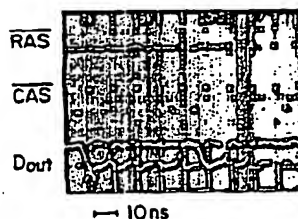
Fig. 19. Observed operating waveforms of the serial READ/WRITE mode.

TABLE I
MAIN FEATURES OF THE EXPERIMENTAL 16-Mbit DRAM

Process technology	Stacked trench capacitor cell
	Twin-tub CMOS
	3-poly/1-Mo-polycide /2Al
	Minimum design rule 0.7μm
Gate length (effective)	NMOS 0.5μm
	PMOS 0.5μm
Organization	4M words x4b
Functional options	Fast serial read/write mode
Power supply	5V (internal 4V)
Chip size	17.5 x 12mm²
Cell size	1.7 x 3.6μm²
Access time	t_{RAC} = 70ns, t_{CAC} = 22ns
Serial cycle time	10ns (100 MHz)
Active current	120 mA (t_{RC} = 190ns, V_{CC} = 5V)
Refresh cycles	2048 cycles /32ms

on-chip interleaved circuitry and a double-input-buffer scheme. The cell array layout centers around peripheral circuits in order to minimize the wiring delays.

The chip obtains a 70-ns RAS access time by using this unique layout, together with the high-speed 0.7-μm STD structure CMOS technology. Using the interleaved circuit and the double-input-buffer scheme, a 100-MHz 2K × 4-bit serial READ/WRITE mode has been successfully realized. A retention time of 1 s at 85°C has been achieved by the STT cell. These new technologies hold promise for realizing 16-Mbit DRAM's.

ACKNOWLEDGMENT

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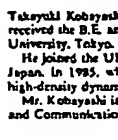
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Synchronous static ram

Using a new static-ram structure featuring a clock input, zero wait-state memory access at 40MHz processor speed is possible with a 25ns device.

DAVID JONES

As microprocessor clock speeds increase, it becomes more and more difficult to design memory capable of keeping up with them. There is no problem with interfacing slow memory systems to the MC68030 microprocessor since the device's asynchronous mode allows wait states to be inserted into memory accesses. But if maximum throughput is needed, memory accesses must be done without these delays.

Traditionally, very-fast static ram has been used to allow memory to be accessed at the speed required by high-performance microprocessors. In the case of a 25MHz 68020 for example static rams with a 25 or 35ns access-time are used. With the 68030 however, access time is reduced still further when the bus controller burst-fills the on-chip caches. Now, data can be accessed in only one clock cycle.

Figure 1 shows a typical microprocessor static-ram design. Although the rams have an access time of only 25ns, control logic required for address decoding, etc., reduces the time available for accessing the devices. As you can see from the diagram, addresses need to be qualified by the address strobe before they can be used to ensure data integrity.

With synchronous static rams, the microprocessor clock feeds directly into the ram access logic to reduce access time. These new memory devices also require less exter-

Fig.1. Standard static ram with edge-triggered latches on inputs and transparent latches on outputs.

Fig.2. Synchronous static ram needs less external control logic than conventional static rams because of its clock input (K). Synchronous devices with 25 and 35ns access times replace expensive high-speed static rams with 5 to 10ns access times.
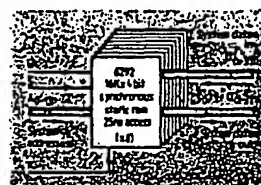
Fig.3. Internal structure of an MCM6292 synchronous static ram. Write-pulse logic required for standard static ram is on chip so fewer external control components are needed.

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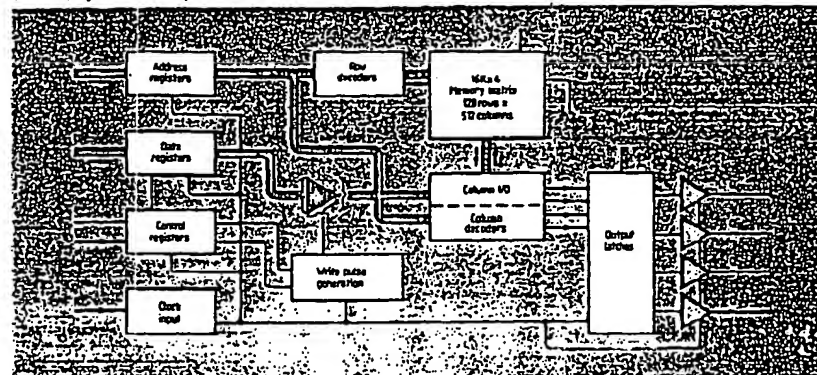
nal logic to interface them to the microprocessor, as Fig.2 shows. Internal elements of the synchronous static ram are illustrated in Fig.3.

Samples of four synchronous ram types will be available from Motorola by the end of this year. The MCM6292 is a 16K×4bit device produced using the HCMOS III process. It has fourteen address inputs, four separate data inputs and outputs, a write-enable line, chip-select input and a clock input designated K.

Operation of the device is as follows. On the positive-going edge of the input clock, all chip inputs including control lines are latched. In addition, when the clock is low, the output latches are transparent (open) and are then held in the correct state when the clock goes high.

If the address and chip-select signals can be supplied with the correct set-up and hold times with respect to the rising edge of the microprocessor clock, data can be read on the next rising edge of the clock. The time between these edges is therefore the cycle time of the memory.

During a write cycle, if the processor can supply address, control and data on the same clock edge then all can be latched together. Complex write-pulse generation logic required with standard ram is now an on-chip function. Figures 4 and 5 show read and write timing for the 6292.

With the exception that its outputs are registered instead of latched the MCM6293 is the same as the 6292. In register-output mode, data that is valid when the clock goes high is from the previous cycle. The MCM6294 and 6295 are the same as the 6292 and 6293 respectively except that they have an output-enable control instead of a chip-select input. These two devices are designed to permit asynchronous control of the output buffers.

It is now possible to build high-performance microprocessor systems with very-fast external caches. In conventional designs, using synchronous static ram is equivalent to using ordinary static rams with 10 to 15ns access times — which are very expensive and of lower density. Synchronous static rams with 25ns access time allow a processor to operate at up to 40MHz without wait states.

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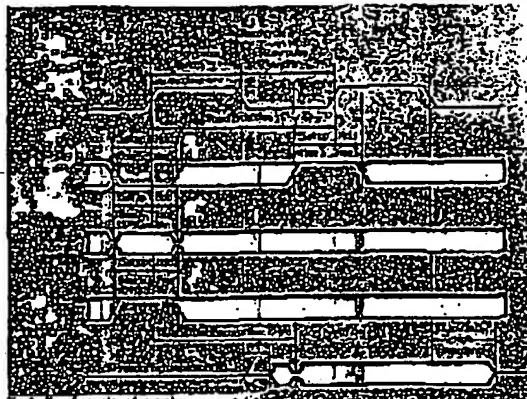
Fig.4. Read cycle of synchronous static ram.
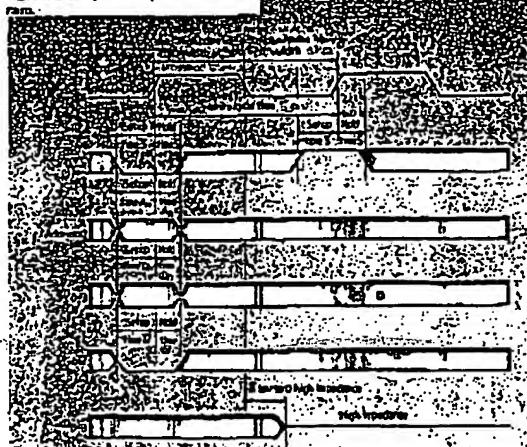
Fig.5. Synchronous static ram write cycle.

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A 1-Mbit DRAM with 33-MHz Serial I/O Ports

KIYOTO OHTA, HIDEKI KAWAI, MASARU FUJII, TOSHIO NISHIMOTO, SEIJI UEDA, AND YUKIO FURUTA

Abstract —This paper describes a 1-Mbit (256K × 4) DRAM with 33-MHz serial I/O ports. High-speed operation, a 33-MHz serial cycle, and a 10-ns serial data access time have been realized by internal serial/parallel conversion circuits, a newly designed I/O controller circuit, new dynamic register circuits, a divided sensing method, and optimized layout design.

The chip is fabricated with a 1.5-µm double-level polysilicon and double-level aluminum N-channel MOS process technology. An optimized interleaved transistor realizes equivalent first- and second-level aluminum pitches for a compact chip design. The chip size is 5.83 × 11.5 mm².

This memory has high-speed input and output capability as well as random accessibility. These features are suitable for TV and VCR frame memory system applications.

I. INTRODUCTION

RECENTLY, digital signal-processing techniques have been applied to TV and VCR systems in order to obtain high picture quality and additional features. In the digital TV or VCR system, field or frame memories are used for storage of the information of complete video fields or frames [1], [2]. A memory of large bit size and fast data rate has been strongly required for this field or frame memory application. In the NTSC system, for example, one field video information is approximately 1.9-Mbit when sampled at 4 f_{sc} (14.3 MHz) with 8-bit resolution. And an approximately 28.6-MHz (8 f_{sc}) data rate is required for a noninterlaced scanning application.

CCD memory [3] and serial-access memory [4] have already been developed for the field memory application. However, they have no random accessibility, and thus are insufficient for further applications. On the other hand, some dual port video RAM's [5], [6] have been developed for the frame buffer application in the graphic display system. However, they are not always suitable for handling the continuous video signal.

In view of the above requirements, we have developed a 1-Mbit DRAM suitable for either field or frame memory application in the digital TV and VCR system. The memory has 33-MHz serial I/O ports and internal serial/parallel conversion circuits. The memory can deal with asyn-

chronous inputs and outputs at a 33-MHz data rate and has random accessibility, which allows wide applicability.

This paper describes the 1-Mbit DRAM with 33-MHz serial I/O ports [7]. In Section II the chip design techniques concerning circuits and layout are discussed. Section III describes the 1.2-µm double-level aluminum NMOS process technology used to fabricate this memory. In Section IV the characteristics of this memory are described and the chip application is also discussed.

II. CHIP DESIGN TECHNIQUES

A. Chip Construction

Fig. 1 shows the chip block diagram of this memory. The memory has an organization of 256K × 4 bits. Each 256-kbit block has two sets of serial/parallel data conversion circuits, which are constructed with 8-bit serial shift registers, for data input and output. The 256-kbit block is divided into eight units, resulting in 32K × 8-bit memory cell arrays. Each array has an I/O controller circuit, which controls the data flow between the 32-kbit memory block and its corresponding shift-in and shift-out registers. This memory is randomly accessible to one of 32-kbit addresses. Eight bits of serial data are associated with each address. Serial data inputs and outputs are controlled by serial-in control (SIC) clock and serial-out control (SOC) clock, respectively. Two clocks, /RS and /WS, control the data transfer operation in the I/O controller blocks. This memory has a 9-bit address counter to refresh the RAM every 512 cycles, and it is controlled by the /RFSH clock. A one row address redundancy circuit is included in this memory.

B. I/O Controller Block

The frame memory for a digital TV or VCR system should be capable of dealing with a continuous video signal input and output stream. In view of this requirement, the I/O controller block needs to be designed to perform continuous data input and output simultaneously. Also, data transfer between the shift registers and the memory block should be executed quickly and smoothly.

Fig. 2 shows a schematic diagram of the I/O controller with data flow between the 32-kbit memory block and
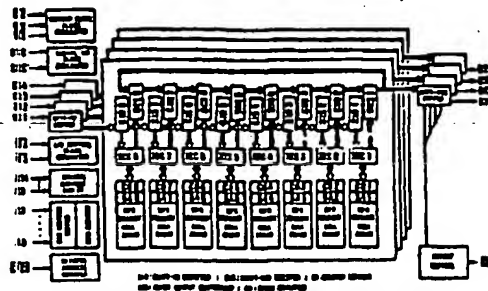
Fig. 1. Block diagram of the memory. Memory cell arrays are divided into four sets of 256-kbit blocks which have an organization of 32K × 1 bit. Each 256-kbit block has an 8-bit serial/parallel conversion circuit.
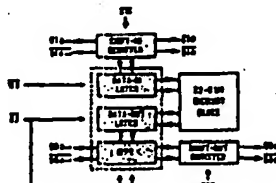
Fig. 2. I/O controller block (enclosed by dotted line) controls data transfer between shift register and memory block.
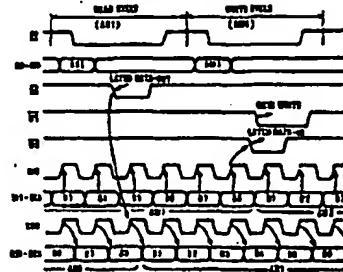
Fig. 3. Timing diagram for the same clock rate READ/WRITE operation. At the falling edge of /WS, input data are transferred to the data-in latch and are written into the memory cell in the following MEMORY WRITE cycle (during low /WS). Readout data from the memory cell are transferred to the data-out latch at the falling edge of /RS.

corresponding shift-in and shift-out registers. The I/O controller block is constructed with a data-in latch, a data-out latch, and a multiplexer to switch data input for the shift-out register. Fig. 3 shows the timing diagram for this memory operation.

The input data carried by the shift-in register are stored on the data-in latch under the control of the /WS clock. The data stored on this data-in latch are written into the memory block in following MEMORY WRITE cycle. Once the data are stored, the data-in latch holds the data and it is unaffected by operation of the shift-in register. The data-in latch allows the data hold time for writing input data into the memory block to be prolonged sufficiently, and permits continued high-speed serial shift-in operation.

The output data from the memory block are stored on the data-out latch under the control of the /RS clock, and then transferred to the shift-out register through the multiplexer. The multiplexer selects either data from the data-out latch or from the previous shift-out register. The data multiplexing is executed smoothly under the control of /RS and SOC clocks. The readout data can be transferred from the memory block to the shift-out register within the minimum serial-out cycle time. Therefore continuous serial data output can be performed, even during the data transfer from the memory block to the shift-out register, with

no change in serial data access time. Furthermore concurrent handling of data-in and data-out can be performed by the I/O controller block with the two clocks /WS and /RS.

C. New Register Circuit

A new type of dynamic register circuit, shown in Fig. 4, is designed to achieve high-speed data transfer operation through the I/O controller block and the shift registers. The register circuit is composed of a set of transfer gates, a comparator to which a dynamic differential amplifier is applied, a buffer, and a latch. Data flow is controlled by three clock phases ϕ_1, ϕ_2, and ϕ_3. In the case of the shift-in register, these clocks are triggered by the SIC clock. Transferred data from the previous register are latched with the clock ϕ_1, and sensed with the clock ϕ_2. The clock ϕ_3 activates the buffers to drive the shift register data bus lines. The latches hold the data during precharge
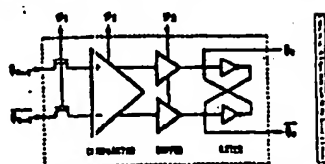
Fig. 4. New type of dynamic register circuit.
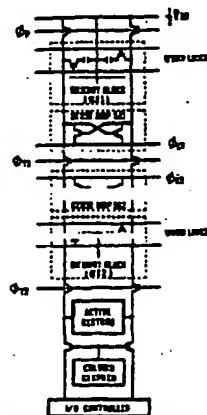
Fig. 5. Circuit diagram of divided sensing method. Bit lines are divided into two parts by transfer gate (gated by ϕ_{Tr}).

Fig. 6. Chip microphotograph. Chip size is 5.83 × 11.2 mm².
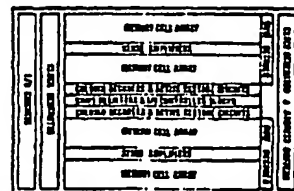
Fig. 7. Physical location of circuit blocks. Shift registers and I/O controller blocks are located at the center of the chip.

cycle of the SIC and SOC. These latches are constructed with an E/E inverter whose load gates are pulled up to a $V_{cc} + \alpha$ level. The delay time from ϕ_1 to ϕ_2 is designed to be approximately 5 ns for typical conditions.

This register circuit with the differential signal handling makes it possible to realize fast and stable operation, in spite of its rather heavy loading capacitance due to the positioning of shift registers. In order to achieve high-speed performance of data transfer between the shift registers and the I/O controller, the output of the comparator is directly connected to the next register input. Furthermore, in order to reduce data access time, the output buffers are directly driven by the last shift-out registers.

D. Sensing Method

This memory employs the divided sensing method, shown in Fig. 5, in order to enhance performance. The bit lines are divided into two parts by transfer gates, which are controlled by clock ϕ_{Tr}. Sense amplifiers are located on both sides of the transfer gates. When the memory block

$MB1$ is selected, readout operation is performed as follows. The selected cell data are read by the sense amplifier $SA1$. The readout data pass through the transfer gate to the memory block $MB2$. Then the data are amplified by sense amplifier $SA2$ and transferred to the active restore circuit. On the other hand, when the memory block $MB2$ is selected, data are read by the sense amplifier $SA2$ and transferred to the active restore circuit without activation of the sense amplifier $SA1$. With this sensing method, the transfer ratio of C_B/C_S for the first sensing stage is approximately 10, which is enough to realize a stable sensing operation.

E. Chip Layout

Fig. 6 shows a microphotograph of this memory chip. Fig. 7 shows the physical location of the circuit blocks in this memory. The chip size is 65.86 mm² (5.83 × 11.2 mm²), and the memory cell array occupies approximately

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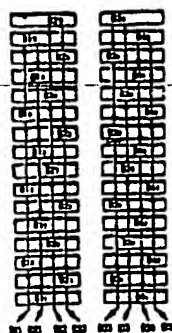
Fig. 1. Connection scheme of shift registers.

54 percent of the chip area. The memory cell array is divided into 64 blocks of 16-kbit per block. A pair of these blocks and the sense-amplifier block between them make up a 32-kbit memory block. The shift-in registers, the shift-out registers, and the I/O controller blocks are located at the center of the chip. Each shift-in register, shift-out register, and the I/O controller block is laid out adjacent to the corresponding 32-kbit memory block. This configuration gives high-speed performance and stable operation of the memory, and provides two additional advantages in circuit design. First, the length of the memory data lines between the memory block and the I/O controller block is minimized in this configuration, which in turn minimizes the array capacitance of the memory data lines and is necessary in obtaining high-speed sensing. Second, the 32 pairs of memory data lines neither cross nor run side by side, thus reducing any coupling interference between them. This configuration is also effective in obtaining stable operation and minimizing pattern sensitivities. Furthermore, the shift register arrangement, shown in Fig. 8, results in equalization of the shift register bus lines and output loading capacitance, and is needed to obtain high-speed and stable serial-in and serial-out operation.

III. PROCESS TECHNOLOGY

This memory is fabricated with 1.2-μm double-level polysilicon and double-level aluminum N-channel MOS process technology. Table I summarizes the key process parameters.

Fig. 9 shows a cross section of the memory cell. The memory cell uses the conventional planar-type capacitor. The cell plate is formed with the first level of polysilicon. Word lines are made with the second level of polysilicon stitched to the second-level aluminum word lines at 15 positions of equally divided length. This word-line structure reduces signal propagation delay caused by wiring

TABLE I
PARAMETERS OF THE 1.2-μm NMOS PROCESS

Process	CMOS
	Double level poly silicon
	Double level aluminum
	LDD Structure
	Improved LOCOS
1st Gate Material	Poly silicon
2nd Gate Material	Poly silicon
1st Gate Oxide	100 Å
2nd Gate Oxide	250 Å
Gate Length	1.2 μm
Aluminum Pitch	3.0 μm
Bit Line	1st Aluminum
Word Line	2nd Poly Si / 2nd Al
Cell Size	4.5 μm × 7.8 μm
Chip Size	5.83 mm × 11.2 mm
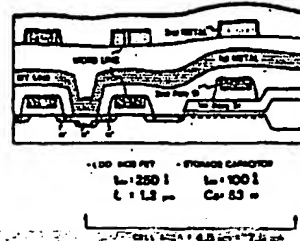
Fig. 9. Cross section of memory cell.

resistance to approximately 1/200 of that for the second-level polysilicon alone. The cell size is 4.5×7.8 μm² (35.1 μm²). A cell capacitance of 55 fF is realized by using a 100-Å gate oxide thickness and an improved LOCOS process. To achieve a highly reliable memory cell, the cell plate is biased to one-half of the V_{cc} level.

The gate oxide thickness for the second-level polysilicon is 250 Å and the minimum gate length is 1.2 μm. An optimized lightly doped drain (LDD) structure is applied to transistors in order to suppress hot-electron injection and thus to suppress degradation of transistor characteristics.

An optimized interlayer insulator fabrication process between the first- and second-level aluminum layers results in a minimum pitch of 3.0 μm for the second-level aluminum interconnections which is the same as the first-level aluminum pitch. This double-level aluminum process technology aids in achieving an effective interconnection layout and in reducing propagation delay times.

Fig. 10. Typical output waveform. At $V_{cc} = 4.5$ V and at room temperature. Vertical: 2 V/div; horizontal: 10 ns/div.

TABLE II
CHARACTERISTICS

Organization	256k × 4 bit
Package	40 pin, 600 mil DIP
Power Supply	5 V ± 10 %
Serial Cycle Time	30 to 60 (Ns)
Serial Access Time	10 ns
Operation Current	100 mA
Stand-by Current	12 mA
Refresh	512 cycle/ 8 ms
	Auto Refresh (RAS)
	Serial Refresh (SRC)
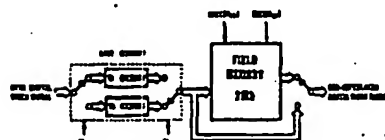
Fig. 11. Schematic of interlaced-to-noninterlaced conversion system. One field size is approximately 2 Mbit for the NTSC system. In the case of 4-f_{sc} sampling and 8-bit resolution. The sampling frequency 4-f_{sc} is approximately 14.3 MHz, and thus 8-f_{sc} is approximately 28.6 MHz.

IV. CHARACTERISTICS AND APPLICATION

A. Characteristics

Fig. 10 shows a typical output waveform with SOC clock. Approximately a 10-ns serial access time is achieved at $V_{cc} = 4.5$ V and at room temperature. Under typical conditions ($V_{cc} = 5$ V and $T_a = 25°C$), and at 33-MHz serial operation, active current is 100 mA and standby current is 12 mA. Typical characteristics of this memory are summarized in Table II.

B. Application

As an example of the application of this memory, a noninterlaced scanning TV application is described. Fig. 11 shows the schematics of an example of the interlaced-to-noninterlaced converting system for NTSC digital video signal sampled at 4 f_{sc} with 8-bit resolution. The sampling frequency 4 f_{sc} is 14.3 MHz, and thus 8 f_{sc} is 28.6 MHz
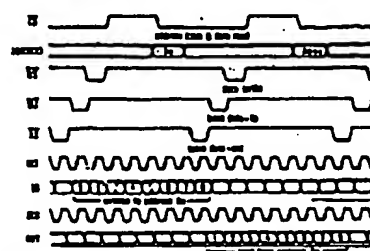
Fig. 12. READ-MODIFY-WRITE cycle timing chart. This memory can execute the READ-MODIFY-WRITE cycle at a 33-MHz data rate. This cycle can be applied to noninterlaced scanning.

for the NTSC system. The field memory, which is constructed with two of these 1-Mbit DRAM's, and a pair of line memories, operating with a 4 f_{sc} input data rate and 8 f_{sc} output data rate, make up the system. The field memory is operated at 8-f_{sc} clock rate for both data-input and data-output. READ-MODIFY-WRITE cycle timings, shown in Fig. 12, are applied to the field memory. A noninterlaced video signal is obtained by alternating the output from the line memory and the field memory.

V. CONCLUSION

A 1-Mbit DRAM with 33-MHz serial I/O ports has been developed with internal serial/parallel data conversion circuits and a newly designed I/O controller circuit. The dynamic register circuit and sensing method offers high-speed stable operation with an optimized layout design. This 1-Mbit DRAM is fabricated with 1.2-μm double-level polysilicon and double-level aluminum N-channel MOS process technology. The memory has many features suitable for TV or VCR frame memory applications.

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The SBus:
Sun's High Performance System Bus for RISC Workstations

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Abstract

A critical element of Sun's recently announced SPARCstation 1 is its memory and I/O expansion bus, which we call the SBus. The SBus is a 32-bit bus that provides the memory bandwidth necessary to provide low-miss-cost access by the CPU as well as low-latency access by I/O devices such as Ethernet and SCSI. The SBus is not a general-purpose backplane bus. Rather it is designed as a direct chip-level interconnect for use on a CPU motherboard and as the interface to I/O expansion cards that plug directly into the motherboard. Interfacing to the SBus requires only 82 signal pins. This modest pin count together with CMOS-compatible signalling protocols and electrical characteristics, makes the SBus ideally suited to today's low-cost CMOS gate arrays, which are the workhorses of low-cost high-performance RISC workstations.

1. Introduction

The SBus is a high-performance device-level bus used in Sun's recently introduced SPARCstation 1 [1]. The SBus is designed to support the performance and cost constraints imposed by a high-volume RISC-based desktop workstation. Important features of the SBus include:

- Synchronous operation.
- System clock speeds ranging from 16.67 MHz to 25 MHz.
- A 32-bit data bus.
- Support for 32-bit Direct Virtual Memory Addressing (DVMA) for SBus masters.
- A 28-bit physical address.
- Burst modes that allow 32 bits of data to be transferred every clock cycle.
- Dynamic bus sizing for 8-bit and 16-bit devices.
- Bus reruns for supporting slow devices.
- CMOS-compatible driving and loading, so that CMOS gate arrays may be connected directly to the SBus.
- Geographical device selection, so that no jumpers are required.
- Programmable device configuration using Forth.

This paper is an overview of the design of SBus. As with most buses there is the issue of what is theoretically possible on the bus versus what happens in a particular implementation, such as Sun's SPARCstation 1. Since the SBus will be used in a variety of Sun systems, this paper describes the SBus generically, and refers to the SPARCstation 1 only to illustrate one of many possible implementations.

2. SBus Design Goals and Features

The process of designing a high-volume RISC workstation requires that the designer carefully balance issues such as time-to-market, the available technology, performance, features and cost. Early in the design of the SPARCstation 1, Sun engineers focused on CMOS gate arrays as the technology of choice. In doing so, it became apparent that the most cost-effective way to implement the system was to have a single high-performance bus that could be used both to connect the processor's cache to memory and as the interface for on-board and plug-in I/O devices.

In creating the SBus, the foremost goal was that overall system performance should not suffer due to the design of the SBus. Since in many systems the SBus would be used as the interconnect between the cache and main memory, it was mandatory that the SBus allow cache-fills to happen as fast as main memory could provide the data. Hence the SBus needed to support peak data rates commensurate with the fast page-mode data rates of current and future dynamic memories.

The next most important goal was that I/O devices, including Ethernet and FDDI, be able rely on the same high-performance, low-latency access to memory that is available to the central processor. The reason that meeting this goal was desirable is that it allows high-performance I/O devices to be implemented without large private buffers, thus substantially lowering their cost.

Another goal was that it be possible to implement the interface between an I/O device and the SBus in a low-cost CMOS gate-array, without having to use external buffers or drivers. This goal was important in that many of the I/O subsystems connect to the system via the SBus. For example, in the SPARCstation 1, the SCSI and Ethernet Direct Virtual Memory Addressing (DVMA) controller, the DRAM controller, and the frame-buffer controller are each implemented as a single chip.

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A final goal was for the SBus to be the interface for I/O expansion. Because the SBus was designed as a motherboard system bus and not as a backplane bus, it was possible to achieve this goal by keeping the physical dimensions of single-slot expansion cards to a modest 3.5 inches by 6 inches. Thus, the SPARCstation 1 can provide 3 SBus expansion slots directly on a motherboard that measures only 8.5 inches by 11 inches, even given that the motherboard contains all of the logic for the entire workstation, including main memory.

The combination of these goals served to reasonably constrain the space of possible architectures for the bus. The performance criteria meant that the bus ought to allow for a system clock of 20 to 25 MHz, since this range is compatible with fast-page mode cycle times of 1 and 4 Mbit DRAMS. At the same time, the desire to use the SBus as the I/O expansion bus, together with the desire for single-chip CMOS I/O interfaces, served to make 25 MHz a reasonable maximum clock frequency, due to overall bus capacitance and the drive ability of typical gate-array output buffers.

3. SBus Design Principles

Meeting the goals discussed above resulted in three major design principles that are reflected throughout the protocols:

1. Synchronous operation. The SBus controller is responsible for generating a fixed-frequency clock in the range of 16.67 MHz to 25 MHz. All signals are sampled on the rising edge of this clock and must be driven such that they meet the SBus setup-time and hold-time requirements, under conditions of worst case skew. SBus interrupts are allowed to be asynchronous; it is the responsibility of the controller to "synchronize" them to the system clock. (See Figure 1.)

2. Active drive. After having been asserted, a tri-state control signal is actively driven to its unasserted state before the source removes its drive. This principle is needed in order to drive the bus using the CMOS output buffers found on typical gate arrays. The alternative of using open-drain signals and pullup resistors would have been too slow and would have resulted in undesirable static power dissipation. (See Figure 2.)

3. No driver overlap. No signal (except open-drain interrupts) is driven by two sources during the same clock cycle. Adhering to this principle guarantees that output drivers never fight. In this way the SBus avoids problems such as unreliable operation and excessive power dissipation. Once again, using open-drain outputs would have been incompatible with low-power CMOS. (See Figure 3.)
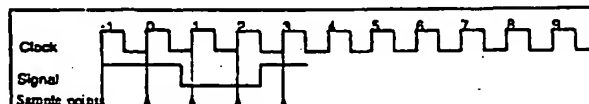
Figure 1. Synchronous operation.
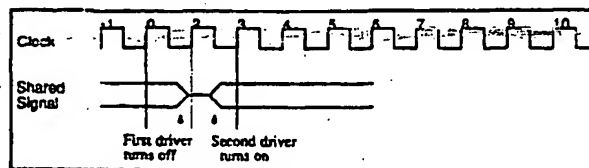
Figure 2. Active drive.

Figure 3. No drivers overlap.

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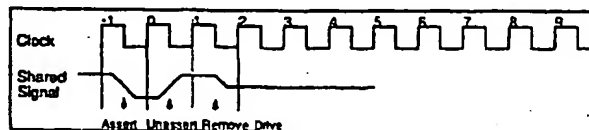
4.   SBus Signals and Expansion Cards.

The SBus uses 82 signal pins for communication. A further 14 pins are used for power and ground in the case of SBus expansion devices. A single-width SBus expansion card is approximately 3.5 inches by 6 inches and connects to the SBus via a 96-pin high-density connector. An expansion device is allowed to load each SBus signal with 20pF of capacitance, and at 20MHz each device must be able to drive a load of 120pF per signal. Finally, each expansion device may draw up to 2 amps at 5 volts.

Table 1 is a summary of these signals.

5.   Typical SBus Systems

As with most system interconnects, the SBus can be used in a number of configurations. The SBus was originally designed with the notion that the CPU was a special participant on the SBus, in that it uses a special path through the SBus controller to gain access to the bus. We call this configuration a host-based SBus. Nominally, SBus masters use the translation hardware in the SBus controller to translate the virtual address that the master has placed on the data lines into a physical address that the SBus controller places on the address lines. The controller then starts the SBus cycle by asserting address strobe, beginning a "slave" cycle. What makes host-based systems special is that due to the CPU's special path, the translation phase of a bus cycle never takes place on the SBus. It is assumed that the CPU has a (logically, at least) private address translation facility.

However, there is nothing that says that the CPU must have this special port. In understanding how the SBus, it is useful to consider "symmetric SBus systems", in which all accesses to the bus, including the CPU's, are DVMA cycles.

5.1 Host-based SBus Systems

A host-based SBus, as shown in Figure 4, is one in which the CPU (for example, a SPARC processor), uses the SBus as its principal memory and I/O bus. In most high-performance systems, the processor will be connected to the SBus via a cache and memory management unit. Depending on exact implementation details, the system bus interface in the cache and MMU may simply be the SBus interface.

As mentioned above, this configuration is the one for which the SBus was originally designed. Because the processor core incorporates the SBus controller, at times the processor appears to be a special SBus participant. Indeed, as will become apparent, the only reason we need to separate an SBus cycle in to a translation cycle and a slave cycle is that in a host-based system, the processor does not use the SBus DVMA mechanism to translate virtual to physical addresses. Rather, the processor uses a direct path to the MMU for this purpose. One reason for implementing systems in this way is that the MMU may want to provide special services to the processor such a larger virtual address space, ability to handle page faults, etc.

Table 1. SBus Signals.

Name	I/O	Description	Driven By
PA(27:0)	I	Physical Address	Controller
D(31:0)	I/O	Data	Controller/Masters/Slaves
Size(2:0)	I/O	Transfer Size	Controller/Masters
Read	I	Transfer Direction	Controller/Masters
Clock	I	Controller Clock	Controller
AddressStrobe_	I	Address Strobe	Controller
SlaveSelect_	I	Slave Select	Controller (one per slot)
Ack(2:0)_	I/O	Acknowledge	Controller/Slaves
LateError_	I/O	Memory Error	Controller/Slaves
Request_	O	Bus Request	Masters (one per master)
Grant_	I	Bus Grant	Controller (one per master)
IntReq(7:1)_	O	Interrupt Request	Masters/Slaves (open drain)
Reset_	I	Reset	Controller
Extension	I/O	Future extensions	Masters/Slaves/Controller
Gnd (7)	PG	Ground	Controller
+5V (5)	PG	Power	Controller (2 Amps per slot, max)
+12V (1)	PG	+ 12 Volt	Controller
-12V (1)	PG	- 12 Volt	Controller
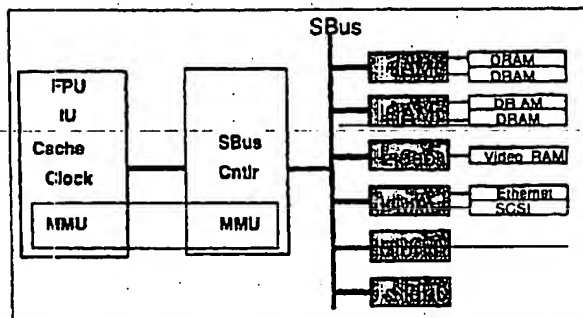
Figure 4. A host-based SBus system. The SBus devices shown are the ones used in Sun's SPARCstation 1. Note, however, that in the SPARCstation 1, the SBus controller is physically part of the Cache and MMU ASICs.
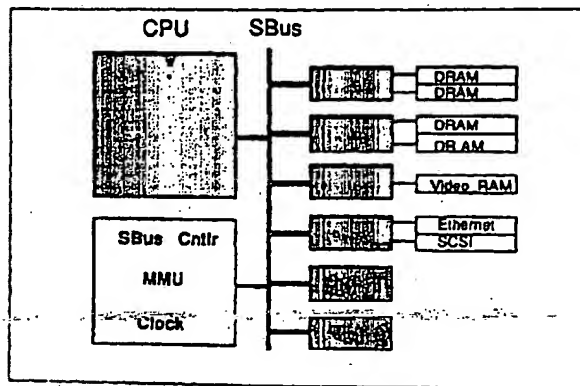
Figure 5. A symmetric SBus system.

In some very high performance systems it may be desirable for the SBus to be used only for I/O, and not as the processor's path to main memory. This configuration may be useful in systems that embody memory buses that are wider than 32 bits. In this case a processor bus to SBus interface will either support bidirectional transfers, or the SBus will need to have local memory, assuming that I/O masters will be on the SBus.

5.2 Symmetric SBus Systems

In a symmetric configuration, as shown in Figure 5, the host CPU is identical to every other master on the bus. In this case, the SBus controller is responsible for all of the centralized functions as discussed above. Note that in this configuration there is nothing that prevents the CPU from having private memory, as well as its own MMU for providing translation services for access to that memory.

6. The Basic SBus Cycle

As illustrated in Figure 6, a complex SBus cycle, which we often call a DVMA cycle, consists of a translation cycle, which results in a physical address being placed on the bus, and a slave cycle which causes data to be transferred between the master and the slave. When the CPU master accesses the SBus in host-based systems, no translation cycle occurs on the bus.

6.1 Translation Cycle

The translation cycle begins when the SBus controller, having detected that some master has asserted Request_, decides to grant bus access to that master. At this time:

- The SBus controller will assert Grant_ for that master.
- On next rising edge of Clock, the selected master will sample Grant_ as asserted and must immediately place a virtual address onto D(31:0) for exactly one clock cycle. The master must also, drive Size(2:0) and Read to their appropriate values.
- The SBus controller will sample this address on the following rising edge of Clock. If the master is writing to the slave, it must put the first word of data onto D(31:0) at this time.
- The SBus controller must then translate the virtual address. When the SBus controller places a physical address onto PA(27:0) and asserts AddressStrobe_, the translation cycle ends and the slave cycle begins.

6.2 Slave Cycle

At the beginning of a slave cycle the bus controller will:

- assert AddressStrobe_,
- drive a physical address onto PA(27:0),
- assert SlaveSelect_ for the designated slave,
- and, in a host-based system, Read, Size(2:0), and D(31:0) (if performing a write), will be driven at this time.

The selected slave then has up to 255 clock cycles to perform the requested transfer and issue a non-idle acknowledgment on Ack(2:0). In the case of a burst transfer multiple acknowledgments will be generated by the slave even though AddressStrobe_ remains asserted for the entire time. After the last acknowledgment, the slave must drive Ack(2:0) back to the idle state for one clock cycle, and in the following clock cycle remove its drive. LateError_ may be asserted by the slave two clock cycles after Ack(2:0) is asserted. In the case of burst transfers a slave that is capable of transferring a word per cycle will leave Ack(2:0) asserted for the each clock cycle a word is being transferred. Slaves that require more time must drive Ack(2:0) back to the idle state during the intervening time. In all cases after the final Data Acknowledge the slave must be certain to drive Ack(2:0) back to the idle state for a cycle, and then remove its drive.
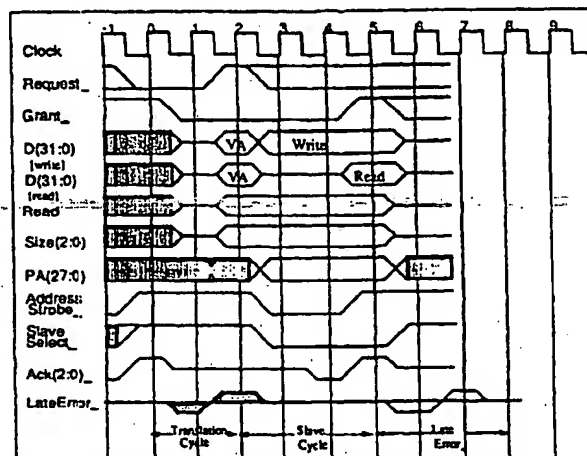
Figure 6. The basic SBus cycle, illustrating both translation and slave portions.

7. Performance and Latency

One of the principal rationales behind the design of the SBus was the desire for high performance. The obvious reason SBus performance is important is that it is an significant element of overall system performance. Less obvious, but a key motivation behind the design, is that having a high performance bus can reduce the cost of bus masters by allowing the masters to have a minimum of private buffer memory. Obviously to realize this capability, a system built around the SBus must include high-performance system memory that is able to satisfy the raw bandwidth requirements of the devices on the bus. Carefully implemented SBus systems should have no trouble keeping up with I/O devices such as FDDI. Of course, since many of these systems will be using the SBus as the CPU's memory bus, system and board designers must consider the impact on CPU performance if a master uses a substantial fraction of the sustained bus bandwidth.

Raw SBus performance is provided by allowing a system clock of up to 25 MHz. Though it might have been possible to design the SBus to run at higher clock frequencies, 25 MHz represents a nice balance between ultimate performance and ease of system design and integration when boards are built by different manufacturers.

Potentially, the SBus can transfer a word every clock cycle. So at 25 MHz, the SBus has a peak data rate of 100 MB/second. The SPARCstation 1 implements a 20 MHz SBus so its peak transfer rate is 80 MB per second. In terms of sustainable transfer rates, the SBus provides for burst transfers of up to 16 words (64 bytes), with the opportunity for one word to be transferred each clock cycle. In the case of a host-based SBus, where a CPU master can overlap address translation with an earlier bus cycle, as few as two cycles of overhead are possible, leading to a burst transfer rate of 64 bytes every 18 cycles or 89 MB/second. In the SPARCstation 1, burst transfers are limited to 16 bytes, and take 11 clock cycles in the case of a CPU access to system memory, resulting in a sustainable burst transfer rate of approximately 29 MB/second.

DVMA masters will incur at least an additional 2 clock cycle overhead for the translation cycle, resulting in a minimum of 20 cycles to transfer 64 bytes, or 80 MB/second at 25 MHz. Once again the inability of a memory system to provide data at this rate may reduce this performance. For example, in SPARCstation 1, only 16-byte burst transfers are supported for DVMA, and such bursts require 13 clock cycles when accessing system memory. Thus at 20 MHz, an SBus master in a SPARCstation 1 can achieve transfer rates of about 25 MB/second when transferring data to or from system memory. Note that the transfer rate in a SPARCstation 1 is limited by system memory, not the SBus per se.

The other important parameter that affects performance is latency. The SBus addresses latency in several ways. First, the maximum length of any slave cycle is 256 clock cycles. A slave that requires additional time to complete a request must use the bus rerun mechanism.

Second, no more than eight bus masters are allowed in any system, and arbitration between these masters is fair. Thus, the absolute worst case latency for a master is approximately 118 μs at 16.67 MHz.

A more likely latency condition in a high-performance system is that on occasion a master may need access to the bus while some other master is accessing a slow slave. In this case, the latency can be slightly more than 256 clock cycles, or 15 μs at 16.67 MHz.

Though some devices may need to be designed for worst-case latency, most I/O devices can be designed based on expected latency. A good example is a device such as an Ethernet controller where system performance depends on having good average case performance, but the system will not malfunction (though a few packets may be lost) if worst-case latency occurs once in a while. Hence, a more typical latency condition is that a master must wait for other masters to complete their SBus cycles to system memory. In the case of SPARCstation 1, the worst expected latency is when four masters are all competing for the bus. (SPARCstation 1 has the CPU, one on-board DVMA master used for Ethernet and SCSI, and two expansion slots capable of supporting DVMA masters.) Assuming that all four devices are accessing main memory, and performing burst transfers, a master will be able to transfer 16 bytes of data approximately every 50 clock cycles (11 + 3*13). At 20 MHz, this results in a transfer rate of 6 MB/second per SBus master, or approximately 24 MB/second aggregate throughput.

8. Conclusions

The SBus is a new kind of system bus that reflects the needs of high-performance RISC-based workstations. The SBus was designed to optimize a number of performance and cost objectives and in doing so:

- Provides high performance at very low cost.
- Takes advantage of modern VLSI technology by allowing low-power CMOS devices to connect to the bus without the need for special drivers or receivers.
- Demonstrates that high performance, expandable RISC machines, can be built at costs that are more typical of PC's than workstations.

By providing low-cost expansion capabilities in their machines, workstation vendors provide opportunities for customers and third parties to add value to their systems. Indeed, the SBus is one of the mechanisms Sun uses to insure that our systems are open. Thus, Sun will be making the SBus available to developers and customers so that they can build expansion cards that connect to machines such as SPARCstation 1.

References

[BeFr 1989] Bechtolsheim, A.V., and Frank, E. H. "SPARCstation 1: Beyond the 3M Horizon," SunTechnology, Vol 2, No 2, Spring 1989, pp. 46-53.

SESSION XIX: HIGH DENSITY SRAMs

FAM 19.2: An 8Kbyte Intelligent Cache Memory

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WITH THE ADVENT OF FINE-LINE fabrication technology and incorporation of pipelining architectures, recent single-chip microprocessors have maximum speed as high as several MIPS. On the other hand, the speed of the system bus is relatively low because of slower main memories.

To fill this speed gap, the use of cache memories in a microprocessor system has become commonplace. Some modern microprocessors have on-chip memories, and one related paper[1] introduced a dedicated chip for the cache memory and memory management unit.

A general-purpose intelligent cache memory with 8Kbyte data memories and support functions, will be reported. Four design goals were: compatibility with most high-performance 16b and 32b microprocessors[2,3,4], no-wait cycles at MPU clock rates of 16MHz or higher, cache-miss ratio of less than 3%, and expandability to a multi-processor system.

The first two requirements require the cache memory to operate at an access time of less than 70ns from address strobe signal to ready signal, and at an access time of less than 83ns from address strobe signal to data valid.

Tradeoffs between including a larger data memory and integrating more control functions in the cache chip were examined by computer simulation to obtain a solution to the cache-miss ratio. Simulation showed that a data memory of more than 8Kbytes should be introduced on one chip, even if sophisticated house-keeping techniques could be adopted. The best approach was revealed to be the combination of a 4-way set associative placement algorithm, 16bytes block size, LRU replacement algorithm, and use of pre-fetch.

The final demand was achieved by separate interfaces for the MPU and system buses, asynchronous operation between both interfaces, and monitoring of the directory memory access via the system bus.

Thus, the cache has been implemented by a high-speed static RAM and is controlled by dual-port directory memories, which allow the cache memory chip to communicate with the MPU while being asynchronously monitored via the system bus.

Figure 1 shows a simplified block-diagram of this intelligent cache memory chip. The data memory at the center is subdivided into four parts of 128 sets x 16 bytes each corresponding to the 4-way set associative placement algorithm.

The address information from the MPU is given to a 27b address interface at the left side, and then compared with the contents of the address TAG memory. The validity is checked in the incorporated valid memory. During a cache-hit or write-cycle, the address information to the main memory is available through the 32b system bus interface at the right side.

Other features and characteristics are shown in Table 1.

Figure 2 shows the waveforms for a cache-hit cycle. The access time measured between the address strobe signal of the MPU and the data valid is 43ns. The ready signal appears at 35ns after the address strobe signal has been given. The minimum cycle time for a hit (read/write) is 60ns. Operating power is 0.7W (typ).

Figure 3 shows operating margins for access time; waveforms for a cache-miss cycle appear in Figure 4.

The chip contains 620,000 transistors in a 13.04 x 13.43mm² die area (Figure 5), and is packaged in a 132-pin PGA. The technology used is a double-metal, polyoxide-gate 1.2µm CMOS process.

Other features include design for testability and parity checks in all the memory functions. Test circuits allow the internal RAMs to be accessed directly and observed. A scan-path scheme is employed in control logic.

[1] Chu, J. and Kahn, J., "A 40K Cache Memory and Memory Management Unit", ISSCC DIGEST OF TECHNICAL PAPERS, p. 50-51; Feb., 1986.

[2] Advanced Information 80386, Intel.

[3] MC68020 32b Microprocessor User's Manual, Motorola.

[4] Ooe, Y., et. al., "A 32b CMOS VLSI Microprocessor with On-Chip Virtual Memory Management", ISSCC DIGEST OF TECHNICAL PAPERS, p. 36-37; Feb., 1986.

Data memory size	8Kbytes (16byte x 128 sets x 4-ways)
Placement algorithm	4-Way set associative
Replacement algorithm	LRU (Least Recently Used)
Block size	4 x 16 bytes (programmable)
Prefetch	Prefetch on miss
Main memory updating	Write-through
Write Buffer	One level
Main memory access mode	Single, burst (programmable)
Main memory access control	Fetch bypass and wrap-around load
Bus system interface	16, 32b (programmable)
Processor interface	16, 32b (programmable)

TABLE 1—Memory features

MPU clock
MPU address strobe
MPU address.
Bus clock
Bus request
Ready signal
System bus I/O
Main memory address strobe
Main memory data strobe
End of cycle
System bus status
MPU Data

FIGURE 4—Waveform for a cache-miss.

MPU address strobe
Ready signal
Data
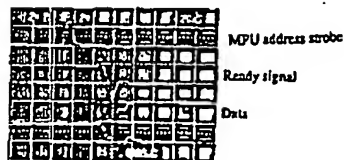
FIGURE 2—Waveform for a cache-hit.
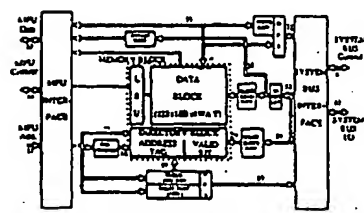
FIGURE 1—Block diagram.

FAIL

PASS

Access time from address strobe to ready signal

VDD
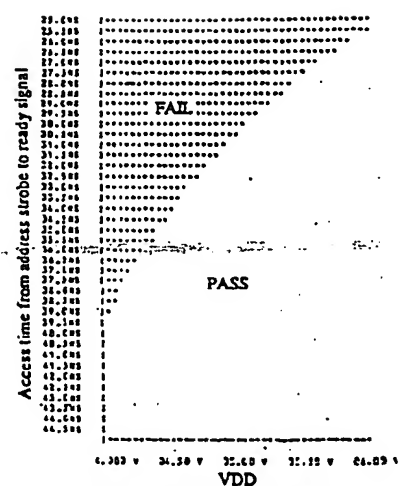
FIGURE 3—Operating margin for access time.

Self-Timed RAM: STRAM

● Chikai Ohno

A STRAM is different from conventional RAMs because it has synchronous operation and an on-chip write pulse generator. Three types of STRAMs are presented in this paper. Each type is a standard device and has unique features which are useful in various applications. A system model using STRAM was evaluated and it was shown that STRAM can improve the system level cycle speed to twice that of a conventional RAM. Using already established process technology, Fujitsu has developed a 1K x 4 standard STRAM having a cycle time of 9 ns and 4K x 4 STRAM having a 13 ns cycle time.

1. Introduction

With the increasing system speed of high-performance data processing equipment, there is a corresponding need for high-speed memory devices. Improvement of the memory speed has mostly been achieved by the introduction of new process technology, but this is becoming increasingly difficult. Even if a high-speed memory device can be developed, it is questionable whether the device performance will be optimized at the system level. For conventional RAMs, timing requirements, including on-board signal skew, and the difficulty of generating a narrow write pulse under a heavy on-board load have made it difficult to improve the system level performance as much as the speed of the memory devices.

For these reasons, the "Self-Timed RAM" (STRAM) has been developed as a synchronous RAM having a new circuit architecture which can improve overall system performance[1]. The STRAM is built using the same process technology as conventional RAMs.

In this paper, the basic structure of the STRAM is described in Chap. 2 and the Latch and Register are defined in Chap. 3. In Chap. 4, three different STRAM configurations and their functions are explained based on the information given in Chaps. 2 and 3. Chapter 5 shows the advantages of STRAM over conventional

RAM by comparing these two types of RAM using a system model. The 1K x 4 and 4K x 4 STRAMs that Fujitsu has developed are introduced in Chap. 6.

2. Basic structure

The basic block diagram shown in Fig. 1 shows that STRAM differs from a conventional RAM in the following ways:

1) STRAM has a circuit which temporarily stores the input and output data

The input buffer gate of each input of the conventional RAM: Address input (ADD), Data input (D_{IN}), Chip Select input ($\overline{CS}$), Write Enable input ($\overline{WE}$), is replaced by a data store circuit in the STRAM. For output, STRAM also provides a data store circuit in front of the output buffer gate.

2) STRAM has an on-chip write pulse generator

Due to the internally generated write pulse, it is no longer necessary to externally control the write pulse width using the $\overline{WE}$ input. $\overline{WE}$ input only provides state information to the RAM whether it is in the read cycle ($\overline{WE}$ = high level) or write cycle ($\overline{WE}$ = low level).

3) STRAM has a clock (CLK) input

The data store circuit and internal write pulse generator for articles 1) and 2) above are controlled by the clock (CLK) input. STRAM has synchronous read and write cycles.

a) Conventional RAM

b) Self-timed RAM
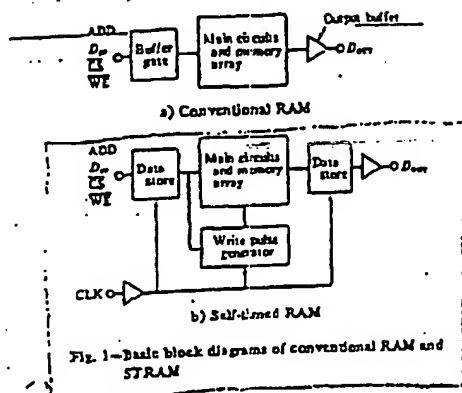
Fig. 1—Basic block diagrams of conventional RAM and STRAM
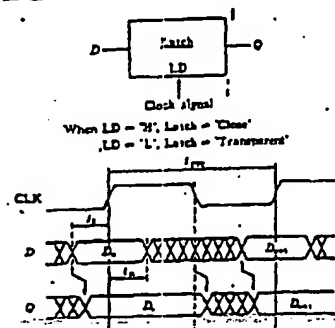
Fig. 2—Latch (Level sensitive type latch).

STRAM variations based on the type of data store circuit are described in the following sections.

3. Definition of latch register

The data store circuits shown in Fig. 1 can be a latch type or register type.

These two types are described below.

1) Latch

The latch defined here is a D-latch type or "level sensitive" type latch. Figure 2 shows that the input data (D) is controlled by the level of the LD input. D is transparent to the output (Q)
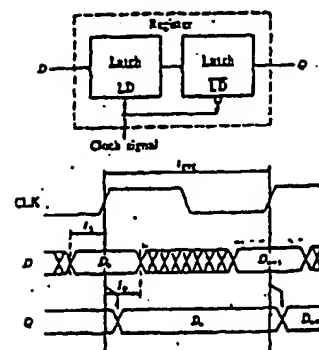
Fig. 3—Register (Edge sensitive type latch).

when the LD input is low (L). The latch is closed and D cannot pass through the latch when the LD input is high (H).

The LD input is controlled by the clock input. Timing references between the external clock input (CLK), input data (D), and output (Q) are shown in Fig. 2. t_S is the setup time and t_H is the hold time of input (D) with respect to the rising edge of the CLK input. These provide the required conditions for the latch to hold the assigned input data.

2) Register

The register defined here is a pair of latches connected in series. One latch is controlled by the LD input and the other by an inverted LD input. Figure 3 shows the timing references between the CLK input, input (D), and output (Q). The register is edge sensitive and controlled by the edge of the CLK input. Therefore, output (Q) remains stable throughout the cycle (t_{CYC}) for the register, unlike the data-through mode for the latch.

These latch and register structures are advantageous for chip layout because the latch or register can be easily built-in using metal option technology. Therefore, the different STRAMs explained in later chapters can be easily manufactured.

4. Types of STRAM

Various types of STRAMs can be manufactured depending on the type of input and output data store circuits. Use of the latch or register explained in the previous chapter is optional for the input and output data store circuits. Figure 4 shows three typical STRAM circuits that are described in this chapter. Figure 5 shows the timing charts of these STRAMs.

1) LL-mode

In the LL-mode STRAM, latches are used for both the input and output data store circuits. The latches are controlled by the internal clock signal. The clock signal to the output latch is inverted. Table 1 lists the input and output latch functions with respect to the CLK input. This table shows that the input latch and the output latch operate opposite to one another. For example, during the high CLK input state, the input latch is closed, the output latch is transparent, and data is read out at the output. Therefore, any change in the input state does not influence the output data. During the low CLK input state, the input latch becomes transparent, and data from the memory cell tries to pass through to the output. However, data read out does not occur before the next high level CLK input because the output latch is closed during that period.

A feature of the LL-mode STRAM access mode is that output data can appear at the output independent of the clock edge when the set-up time for address inputs is controlled to a relatively small value. This through-mode access (t_{ALADD}) shown in Fig. 5 is the same as the address access time of a conventional RAM.

In the write cycle, write operations must be completed during the high CLK input state only when the address data is fixed in the latch as explained in Chap. 3. Both read and write operations of the LL-mode STRAM are performed

Table 1. Input and output latch operation in LL-mode STRAM

CLK input	Input latch	Output latch
'L'	Transparent	Closed
'H'	Closed	Transparent
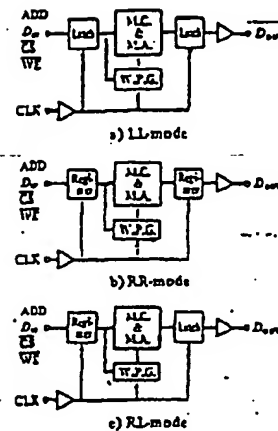
Fig. 4—Types of STRAM.
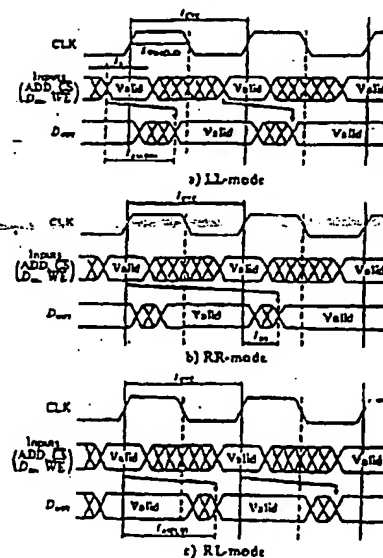
Fig. 5—Timing charts of three types of STRAM.

Table 2. Summary of features of three types of STRAM

Types / Items	LL-mode	RR-mode	RL-mode
Clocking	Min required time to guarantee complete read or write operation during high CLK input high state.	Duty ratio free	Duty ratio free
Read cycle	Address access mode identical to the conventional RAM address access time (t_{AA}) is possible.	Data is available in the next CLK cycle, but high-speed access from the CLK edge is implemented.	Data is available in the same CLK cycle, but it is an access mode from the CLK edge.
Write cycle	Write operation is executed only for a CLK high state.	Write operation can be executed throughout the cycle.	Write operation can be executed throughout the cycle.

during the high CLK input state. Thus, there is a minimum required time for the CLK input high duration ($t_{WH(CLK)}$).

2) RR-mode

The RR-mode STRAM uses registers for both the input and output data store circuits. A feature of the register, as stated in Chap. 3, is that both holding the input data and reading the output data are controlled by the CLK input edge, but the output data corresponding to specific input data does not become available due to the same CLK edge. In a RR-mode STRAM, the read out data is available in the next cycle as shown in Fig. 5. High-speed read operation is enabled because there is only a delay in the output register (t_{DR}) without going through the memory cell array.

In the write cycle, unlike the LL-mode, there is no minimum required time for $t_{WH(CLK)}$ to guarantee the complete write operation because input data remains stable throughout the cycle.

As stated above, duty ratio free CLK input is enabled in the RR-mode STRAM because read

and write operations are initiated by the CLK input edge.

3) RL-mode

The RL-mode STRAM uses a register for the input data store circuit and a latch for the output data-store circuit. Holding the input data and the write cycle is the same as for the RR-mode. It is different from the RR-mode STRAM in that output data is available in the same CLK cycle because the output latch is transparent during the low CLK input state. This is shown in Fig. 5.

Duty ratio free CLK input is also enabled in the RL-mode STRAM as in the RR-mode STRAM.

The main features of these three types of STRAMs are summarized in Table 2.

5. Comparison between conventional RAM and STRAM in a system model

To verify the advantages of STRAM over a conventional RAM on the system level, they were both applied in the system model shown in Fig. 6 and evaluated. Figure 6 shows a system model in which several RAM arrays are controlled by the CPU. The CPU driver generates an Address signal, $\overline{CS}$ signal, D_{IN} signal, and $\overline{WE}$ signal which are conveyed to each RAM array. These signals are generated synchronously by the system clock signal. Read out data from each RAM array is returned to the CPU and is held in the latch. This chapter compares the conventional RAM and STRAM for read cycle performance and write cycle performance when each device is used as the RAM array in this system. The LL-mode STRAM was used in this comparison. The same comparison can be made using the other two types of STRAMs. For simplification, clock skew and skew between the system clock and STRAM clock are ignored here. Only the essential signals required to understand system operation are considered.

1) Read cycle for conventional RAM

Figure 7 shows the timing diagram when conventional RAM is used in the system model. Address signals forwarded by the system clock run along the signal transmission paths to reach

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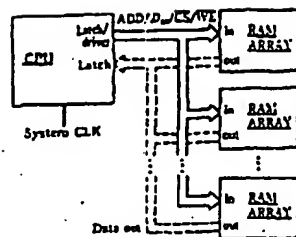
Fig. 6—Memory system model.
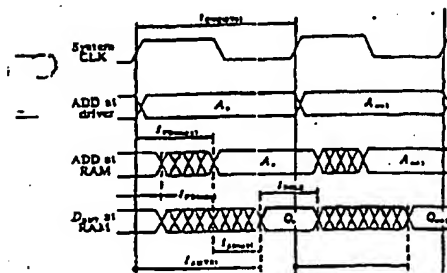
Fig. 7—System read cycle for conventional RAM.

a RAM array in $t_{PD(min)}$ for the fastest case and $t_{PD(max)}$ for the slowest case.

This propagation distribution mainly occurs due to the following factors:

    i) Each RAM has a different length signal transmission path from the CPU.

    ii) Input capacitance of the RAM varies between the maximum and minimum values.

    iii) Speed of the CPU latch and CPU driver also have maximum and minimum values.

    iv) The unit speed of the signal transmission path itself has a certain distribution.

by the system clock, RAM output data becomes valid after the skew between the RAM minimum access time ($t_{A(min)}$) corresponding to the fastest address signal ($t_{PD(min)}$) and the RAM maximum access time ($t_{A(max)}$) corresponding to the slowest address signal ($t_{PD(max)}$). In Fig. 7,

$t_{A(min)}$ is assumed to be zero for simplification. After the RAM output becomes valid, it must be held at the output for a certain period of time so that the CPU can latch the data. This time is called t_{HOLD}.

The system cycle time ($t_{CYC(SYS)}$) for conventional RAM is expressed as follows.

$$t_{CYC(SYS)} = t_{PD(skew)} + t_{A(max)} + t_{HOLD},$$

where $t_{PD(skew)}$ is the skew of signals transmitted in the system and is given by $t_{PD(max)} - t_{PD(min)}$.

As an example, we applied the following assumptions to estimate the actual read and write cycle times in our system.

$t_{PD(skew)} = 10$ ns:

The transmission skew from the CPU to each RAM and from each RAM to the CPU is assumed to have the same value.

$t_{A(max)} = 10$ ns:

A RAM having an access time of 10 ns is assumed.

$t_{HOLD} = 13$ ns:

A RAM output valid time of 3 ns is assumed for the CPU to latch the data from each RAM. Thus, a data hold time of 13 ns is required for the RAM because of the previously assumed 10 ns transmission skew ($t_{PD(skew)}$) from the RAM to the CPU.

Based on these assumptions, the system cycle time is as follows.

$$t_{CYC(SYS)} = 10\ ns + 10\ ns + 13\ ns = 33\ ns$$

Although these values partly depend on each system design, this result implies that RAM having an access time of 10 ns is degraded to about a three times slower cycle time in the system.

2) Read cycle for LL-mode STRAM

The system cycle time when a STRAM is used in the same system is evaluated below. Figure 8 shows the timing diagram. The address signals are conveyed to the STRAM with the same skew as assumed for the conventional RAM. After the STRAM clock edge is inserted within the required setup time (t_S) and the address data is latched in the STRAM, RAM output data is read out within the address access time during the high CLK input state. When the CLK input goes low after $t_{A(max)}$, (i.e. after the output data becomes valid) the
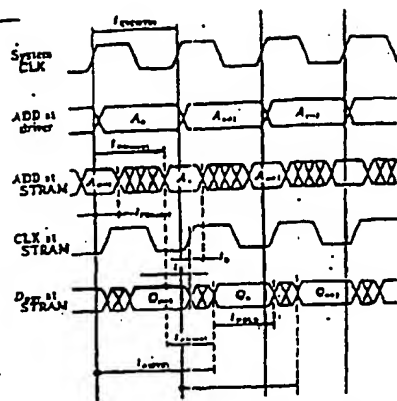
Fig. 8—System read cycle for LL-mode STRAM.

Fig. 9—System write cycle for conventional RAM.

data remains on the output for the data hold time (t_{HOLD}) because the output latch is closed. When the CLK input is high, the input latch is closed. Thus, address signals can be changed to prepare for the next address after the required hold time (t_H) expires.

Based on the functions described above, the system cycle time for the STRAM is expressed as follows.

$$t_{CYC(SYS)} = t_{A(max)} + t_{HOLD} - t_S,$$
or,
$$t_{CYC(SYS)} = t_S + t_H + t_{PD(skew)}.$$

The equation having the larger value dominates the cycle time. A smaller value of t_H can shorten the cycle time as indicated by the latter equation. t_S affects the cycle time calculation in opposite ways for the two equations. If we assume $t_{H(min)} = 2$ ns and $t_{A(max)}$, t_{HOLD} and $t_{PD(skew)}$ have the same values as for the conventional RAM, we can obtain the optimum t_S which minimizes the cycle time for both equations. That is,

$$t_S = 5.5 \text{ ns}.$$

Using this value, the system level cycle time for the LL-mode STRAM is as follows.

$$t_{CYC(SYS)} = 10 \text{ ns} + 13 \text{ ns} - 5.5 \text{ ns} = 17.5 \text{ ns}.$$

As described above, using STRAM can result in a faster system cycle time than conven-

tional RAM under the same system conditions. Although these two types of RAMs have similar system access time ($t_{A(SYS)}$) as shown in Figs. 7 and 8, STRAM can improve the system cycle time due to the timing overlap feature that enables the address to be changed before system access becomes available.

3) Write cycle for conventional RAM

Figure 9 shows the write cycle timing diagram for conventional RAM when address signals and the $\overline{WE}$ signal are transmitted to each RAM with the same amount of signal skew. It is well known that for write cycle timing in a conventional RAM, the required conditions for the address signal setup time ($t_{SA(min)}$) and hold time ($t_{HA(min)}$) with respect to the $\overline{WE}$ signal and minimum pulse width ($t_{VW(min)}$) of the $\overline{WE}$ signal must be guaranteed. To meet these conditions in the system, the following timing conditions must be met (see Fig. 9):

i) $t_{SA(min)}$ during $t_{PD(min)}$ of $\overline{WE}$ signal after $t_{PD(max)}$ of the address signal

ii) $t_{HA(min)}$ during $t_{PD(min)}$ of the address signal after $t_{PD(max)}$ of $\overline{WE}$ signal

iii) $t_{VW(min)}$ between $t_{PD(min)}$ and $t_{PD(max)}$ of $\overline{WE}$ signals

The system cycle that satisfies these conditions is expressed as follows.

$$t_{CYC(SYS)} = t_{CYC(device)} + 3 \times t_{PD(skew)},$$

the $t_{CYC(device)}$ is the write cycle time of each

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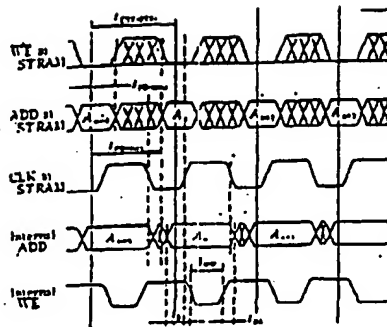
Fig. 10—System write cycle for LL-mode STRAM.

Fig. 12—4K x 4 STRAM chip (6.1 mm x 4.5 mm).
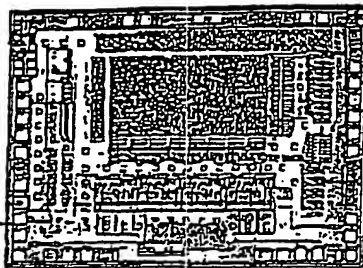
Fig. 11—1K x 4 STRAM chip (4.5 mm x 3.3 mm).

RAM. It is given by $t_{SA(min)} + t_{WW(min)} + t_{HA(min)}$. Let us assume that $t_{CYC(device)}$ is 10 ns.

$$t_{CYC(SYS)} = 10 ns + 3 \times 10 ns = 40 ns.$$

This indicates that the system level cycle time can be as much four times that of the device level. As the device performance is improved, the ratio of signal skew in the total system cycle time becomes larger. The other problem associated with the write cycle time of high-speed conventional RAM is the difficulty in generating a narrow write pulse width under a large load in the system. Even if this is possible, it is very expensive.
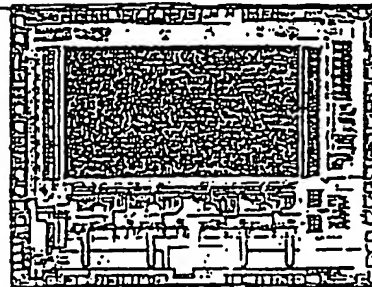
4) Write cycle for LL-mode STRAM

The timing diagram shown in Fig. 10 shows that the skew of the address signals and $\overline{WE}$ signal can overlap because the $\overline{WE}$ signal is held at the STRAM CLK input edge in addition to the address signals. Immediately after receiving the low $\overline{WE}$ signal, the internal pulse generator automatically starts operating to guarantee an internal write pulse that satisfies the required conditions for the internal setup time and hold time with respect to the address signals. These operations are implemented during the CLK input high state with respect to the internal Address and $\overline{WE}$ timings as shown in Fig. 10. The LL-mode STRAM write operation can be completed within the same CLK input high state period as the read cycle because a general characteristic of RAM devices is that $t_{WW(min)}$ is almost the same as $t_{A(min)}$. This means that STRAM enables a write cycle time equivalent to the read cycle time. Using the values previously obtained as the STRAM read cycle time, $t_{CYC(SYS)}$ of the STRAM write cycle can be expressed as follows.

$$t_{CYC(SYS)} : WRITE = t_{CYC(SYS)} : READ = 17.5 ns.$$

As mentioned before, use of STRAM reduces the system level write cycle time to less than half that of conventional RAM.

6. Development of 1K x 4 and 4K x 4 STRAM

Figure 11 is a die photo of a 1K x 4 STRAM and Fig. 12 is a die photo of a 4K x 4 STRAM.

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Top view   Top view

a) 1K x 4 STRAM   b) 4K x 4 STRAM
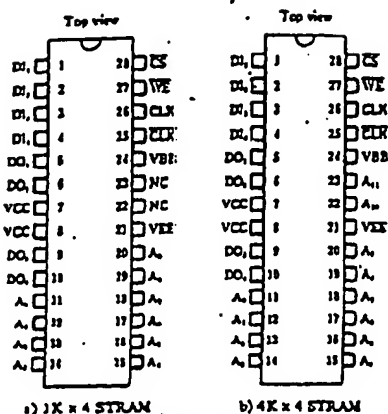
Fig. 13—Pin assignments.

Based on this die, three variations for the LL-, RR-, and RL-modes can be manufactured using metal option technology. Both 10K ECL I/O and 100K I/O can be supported for each mode. Figure 13 shows that the pin configuration is common to each mode. Expansion from 1K x 4 to 4K x 4 is possible.

Two CLK input pins can implement high-speed clocking by using the CLK input and $\overline{CLK}$ input simultaneously in the differential mode. Single-ended mode of the CLK input or $\overline{CLK}$ input is also possible by connecting $\overline{CLK}$ or CLK to the internal reference voltage ($\overline{VBB}$).

The process technologies used are the currently mature IOP-II (Isolation by Oxide and Polysilicon) technology and 1 μm lithography.

The main characteristics for the LL-mode STRAM are listed in Table 3.

Table 3. Main characteristics of 1K x 4 and 4K x 4 LL-mode STRAM

Parameter	Symbol	1K x 4 STRAM	4K x 4 STRAM
Cycle time	t_{CYC}	9 ns min	13 ns min
Clock pulse width high	$t_{WH(CLK)}$	6 ns min	10 ns min
Address access time	$t_{A(ADD)}$	7 ns max	10 ns max
Power supply current	I_{EE}	−380 mA min	

7. Conclusion

This paper introduces STRAM as a RAM having a new circuit architecture that can provide higher performance in the system than conventional RAM. This is achieved by adding relatively simple on-chip latch or register circuits and a write pulse generator using the same process technology. A system model is used to show that STRAM can improve the system cycle speed by more than twice that of conventional RAM. Thus, we can expect that STRAM will be widely used as a standard device in the future as a substitute for conventional RAM. STRAM will gain a reputation as an indispensable technology especially for higher-speed RAM devices because STRAM can avoid signal skews that are becoming a major factor in limiting the improvement of system performance[3].

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FAST PACKET BUS FOR MICROPROCESSOR SYSTEMS WITH CACHES

Increased microprocessor performance requires increased processor-to-memory bandwidth. The addition of a cache with a line size greater than one offers the highest processor performance at the cost of still higher bus bandwidth requirements. A fast local bus is defined that allows packetized transfers that both maximize memory subsystem efficiency and minimize processor delay during a cache line reload.

In microprocessor systems the processor needs to access memory for both instructions and data. The access time of memory is inversely proportional to the cost of the memory - fast access memory is available at higher cost than slower memory. A frequent solution is to provide a small amount of high cost fast memory and a large amount of lower cost memory. The small, fast memory is called a cache. The performance of the system is usually directly related to the memory subsystem average access time. The average access time is equal to the percent of time the cache memory is accessed (its hit rate) multiplied by its access time plus the miss rate multiplied by the access time of main memory. The hit rate of a cache can be increased by either increasing its size (and cost) or using a larger line size.

The cache line size is the number of bytes that are reloaded every time the cache has a miss. Since processors have a locality of reference, the neighboring words of the missing word have a high probability of being required by the processor in the near future. One disadvantage of providing a line size greater than the system bus width is that it increases the number of transfers across the system bus compared to a line size equal to the system bus (because some of the neighboring words will not be accessed and would not have been loaded into the cache in normal operation). The larger line size has an overall performance benefit if the cache reloads do not exceed the system bus bandwidth.

A standard bus transfer takes two parts: the address portion of the transfer and the data portion. The address specifies where in memory to perform the load (store), and the data provides the existing contents of the memory location in the case of a load or contains the new contents of the location in the case of a store. The overall bus bandwidth can be increased if the transfers are packetized - one address portion is followed by several data transfers with an understood address for the "extra" data words. This is especially suitable for dynamic memories operating in page mode. Page mode is a higher bandwidth method of using the dynamic memory modules that allows faster access to the memory locations when only a subset of the address changes (typically the row address of the array remains constant while the column address can change). Using packet mode, the master on a bus

can specify a number of words in a row, aligned on the word boundary
corresponding to the size of the packet. The memory controller (slave
on the bus) then uses page mode to deliver the resulting data words as
quickly as possible. By aligning the packet on its packet size, the
packet is guaranteed to reside within the same row of the memory array
so page mode can be used. Without packetizing the request, the memory
controller cannot use page mode unless it checks each incoming address
to ensure it is in the same row as the previous address. The time
required to compare each address as it comes in slows down the memory
accesses (even if the memory stays in page mode).

Simply combining a cache with a line size (resulting in higher hit
rates) with a packet transfer mode on the system bus (resulting in
higher bus bandwidth) may not increase the overall system performance
as expected. The problem arises when the desired word in the cache
line is not the first word in the packet. In that case, the processor
must "wait" until the desired word in the packet arrives at the pro-
cessor. With a packet size of 16 bytes (four 32-bit dwords) the pro-
cessor may have to wait for the completion of three dword transfers
before the fourth dword arrives and it can continue processing. If the
packet mode is not used, then the cache can directly request the dword
it is waiting for, but then the overall bus bandwidth increase gained
by packet mode is lost.

A packet mode compatible with different cache line sizes allows
the use of a packet transfer mode during cache line reloads without
reducing the processing performance of the system. This is accom-
plished by allowing the processor (or cache controller) to specify the
starting byte in every packet transfer as well as the size of the
packet. Then the memory subsystem supplies the desired word first so
the processor can resume operation. Following the desired word, the
rest of the packet is transferred from the memory. In order for a
packet mode to work, the order of the words in the packet must be known
by both the processor and the memory controller in advance. In a pre-
ferred implementation, the first word is followed by the subsequent
ascending addressed words in the packet until the last word (highest
address) in the packet is supplied. Then the beginning words in the
packet are supplied until the word that is one less than the requested
first word is transferred. Table 1 on the following page gives several
sample packets of different sizes as well as starting word addresses.

Once the general order of words in a packet is known, the size of
the packet can be altered dynamically. Dynamic packet sizing allows
processors with different cache line sizes to coexist. Another use of
dynamic packet sizing is it can then be used for any bus transfer
larger than a word - array, large datatypes, DMA transfers, etc.

The advantages of the described system are as follows:

Packet Size	First Word	Subsequent Words						
1	0	-	-	-	-	-	-	-
2	0	1	-	-	-	-	-	-
2	1	0	-	-	-	-	-	-
4	0	1	2	3	-	-	-	-
4	1	2	3	0	-	-	-	-
4	2	3	0	1	-	-	-	-
4	3	0	1	2	-	-	-	-
8	0	1	2	3	4	5	6	7
8	1	2	3	4	5	6	7	0
8	2	3	4	5	6	7	0	1
... 8	7	0	1	2	3	4	5	6

TABLE 1

1. A microprocessor packet bus with dynamic packet sizes that inform the system memory controller of how many bytes are in the packet so the memory controller can maximize memory and system bus bandwidth.

2. A microprocessor packet bus as set forth in 1 above wherein the specification of the starting byte within the packet can be made such that the packet size of N bytes, the starting byte m will be followed by the next N-m bytes in ascending order and then starting over at the aligned 0 to m-1 bytes.

3. A microprocessor packet bus as set forth in 1 above wherein the starting byte within the packet is specified by the normal low order address lines.

4. A microprocessor packet bus as set forth in 1 above wherein the size of the packet is specified by a plurality of signal lines on the system bus. These signal lines also allow the coexistence of a packet supporting masters with non-packet supporting masters. The packet size signals default to 1 whenever the master does not assert a packet size.

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FAST PACKET BUS FOR MICROPROCESSOR SYSTEMS WITH CACHES - Continued

5. A microprocessor packet bus as set forth in 1 above wherein the
    packet transfer can be preempted by setting the packet size to a
    minimum value anytime during the packet transfer. When the packet
    transfer is preempted, the sub-transfer in progress is considered
    the last sub-transfer of the packet.

6. A microprocessor packet bus as set forth in 1 above wherein there
    is a packet acknowledge signal on the system bus allowing the
    coexistence of packet-supporting slaves with non-packet-supporting
    slaves. The use of the packet acknowledge signal allows a slave
    to signal to the master if it intends to perform a packet trans-
    fer.

Scalable Coherent Interface*

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Abstract

The Scalable Coherent Interface project (formerly known as SuperBus) is based on experience gained during the development of Fastbus (IEEE 960), Futurebus (IEEE 896.1) and other modern 32-bit buses. SCI goals include a minimum bandwidth of 1 GByte/sec per processor; efficient support of a coherent distributed-cache image of shared memory; and support for segmentation, bus repeaters and general switched interconnections like Banyan, Omega, or full crossbars.

SCI abandons the immediate handshake characteristic of the present generation of buses in favor of a packet-based protocol. SCI avoids wire-ORs, broadcasts, and even ordinary passive bus structures, except that a lower performance (1 GByte/sec per backplane instead of per processor) implementation using a register insertion ring architecture on a passive "backplane" appears to be possible using the same interface as for the more costly switch networks.

This paper presents a summary of current directions, and reports the status of the work in progress.

Introduction

SuperBus was the working name adopted by a Study Group under the auspices of the Microprocessor Standards Committee of the Technical Committee on Mini and Microcomputers in the IEEE Computer Society. The SuperBus Study Group began work in November 1987 under the leadership of Paul Sweazey of National Semiconductor. Its charter was to consider the need for and feasibility of a very high performance "backplane bus," to be at least an order of magnitude more powerful than the existing standard buses.

A consequence of the physical and logical constraints such a system must meet in order to be successful was the new name, SCI (Scalable Coherent Interface), because it became clear that traditional bus structures would not be able to meet the demands of the next decade: the real goal is to interconnect many powerful processors productively, so that the total power of a system can be increased by merely adding more processors.

Our examination of the needs for compute power to handle real engineering problems (e.g. aerodynamic simulation or simulation of large circuit designs) or physics problems (e.g. event reconstruction in the Superconducting SuperCollider) showed that a single bus, even at 1 GByte/sec, would be completely

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inadequate. Many buses (segmentation for parallelism) joined by selective repeaters would be necessary. Or, better yet, no buses at all, but rather some more general interconnection mechanism.

Many architectures which would be perfectly satisfactory for a single bus become ugly, inefficient or impractical for assemblages of multiple buses; i.e., they do not scale well. Thus "Scalable" reflects our constraint that the system be smoothly extensible.

"Coherent" refers to our requirement for a distributed cache-memory coherence mechanism, similar in concept to that developed for the Futurebus, which can greatly reduce the performance cost of interprocessor communication.

"Interface" reflects the generality of our specification, which permits a given module to connect to an unspecified generalized interconnection mechanism, which might be a switching network of any of various kinds, a passive "backplane" forming a register insertion ring, or conceivably even an active bus (i.e. transceivers directly on the backplane).

The SCI standardization project was authorized by the IEEE Standards Board in October 1988, and was assigned the number P1596.

Conventional Buses Are Near their Limits

Present bus systems are running close to physical limits: one cannot speed them up much by turning up the clock frequency or increasing transceiver speed or power, unless one shortens them correspondingly. For example, the Next machine uses NuBus (IEEE 1196) protocols at 25 MHz, 2.5 times the 1196 clock rate, but allows only four sockets instead of the 1196's sixteen. If a bus is short enough and is lightly loaded, transceiver and logic speeds do dominate among its various limits, and so its clock rate can be increased.

The fundamental physical limits are the speed of light, which limits the propagation velocity of signals and thus adds delay to handshakes; the capacitance of connectors and transceivers, which so disturb a bussed signal transmission line that the "ideal transmission line model" is a very poor approximation indeed; and skew, differences in propagation time among a number of parallel signals which threatens to blur the boundary between successive data items.

Other physics problems, such as crosstalk between adjacent signals, are much easier to deal with and have become more economic than fundamental. Distribution of power and ground

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(nontrivial in the face of very rapid changes of current flow) is also in this category, and so is cooling.

Multiprocessor systems have other inherent problems. For example, when many processors operate in parallel to solve a given problem, they need to be able to communicate efficiently with one another in order to share resources or to divide the work. This intercommunication can be a significant bottleneck, perhaps using a large fraction of the system bandwidth just accessing one shared semaphore variable over and over.

Furthermore, fast processors require fast local storage, so they need their own local copies of data, some of which needs to be shared. These local "cached" copies create logical problems if they are modified, because the various copies can become different or incoherent. Somehow, when one processor modifies data which other processors are using, the other processors have to be notified that their local copies are no longer valid so that they can get a fresh copy.

The cache coherency mechanism developed for Futurebus (and now being adapted to Fastbus) requires each cache controller to observe all other traffic in the system in order to determine whether some of its own data might affect or be affected by the current bus operation. Such a "Snoopy Cache" scheme cannot be generalized to highly parallel systems, though it may still be useful for implementing islands of coherency, which may then intercommunicate via more explicit mechanisms such as message protocols.)

SCI Avoids these Limits

Futurebus and Fastbus have gone about as far as is feasible in the use of shared transmission lines which form buses. The most practical way to do better would be to use an active backplane, which has transceiver chips connected directly to the bus transmission lines with no connectors or stubs between. This would minimize the capacitance, and would result in uniform and constant loading which would make it possible to compensate for the loading and significantly improve the transmission line behavior. The connectors would be between the modules and the transceivers, so the presence or absence of a particular module would have no effect on the transmission line loading.

An active backplane scheme could also make live insertion and removal feasible, if module power is controlled by the backplane. However, most customers find the active backplane frightening because of the difficulty of replacing it if a failure should occur and thus it has received little support so far.

Not all backplane physics problems are solved by the active bus mechanism: the wire-OR glitch would still create delays whenever multiple drivers are permitted to be active on a single line, and bus turn-around (changing from one driver to another, as when changing from read to write or when changing mastership) would require delays for similar reasons.

A bus is inherently a bottleneck because it is shared by too many processors. Processor throughput is so high even today that a few processors can saturate any bus. Heavy loading subjects the users to long waits, slowing the whole system.

Therefore SCI intends to abandon the bus mechanism in favor of high speed unidirectional links. Two models are being supported for using these links. The high performance (and high cost) model uses the links to communicate between the module and a fast switch network, resulting in one GigaByte/sec per module.

A lower performance model connects the input and output links of adjacent modules to form a register insertion ring, which can be implemented in printed wiring on a passive backplane structure at low cost but results in only one GigaByte/sec throughput per backplane.

Even this low-cost version is much faster than any existing backplane bus system, so it seems attractive especially as a transition model for the short term while processors proliferate and costs decrease.

We expect to standardize on one module which can operate equally well in either environment, so that processors from many vendors can be developed and used effectively in small quantities at first, and then be moved into a switch environment unchanged when switches become available or necessary or economical for the given application.

This provides a nearly unbounded upgrade path for system growth, and should create an attractive market for the manufacturer (high volume) and for the user (low cost due to high volume and competition among manufacturers).

Unidirectional links effectively remove the speed-of-light barrier to system growth: the system size and clock rate are decoupled, and there are no cycle-by-cycle handshakes. Physical signalling problems are greatly simplified because there is always one driver and one receiver, at opposite ends of the link.

Signals operate steadily whether there is data flowing or not, which makes it easy to use phase locked loops for data extraction if desired (there is no start-up preamble required). That would make it possible to eliminate skew completely by encoding clock timing with each data bit transmitted, although we do not think this will be necessary yet at our initial 1 GigaByte/sec transmission rate.

A central clock will be distributed as a frequency reference so that only phase differences have to be compensated during data extraction. Differential signalling, probably ECL but perhaps current-steering drivers instead, results in constant current flow between connected modules, enormously simplifying the ground distribution problem compared to normal buses.

We plan to use a narrow 16-bit data path at 2 ns/word (250 MHz clock, both edges active), to control the interface IC pin-count problem and make switch elements more practical. Note that 'differential' implies 2 pins per signal, and 'unidirectional' implies 2 links, one for input and one for output, so we are talking about 64 pins minimum for each SCI interface circuit just on its fast end. A circuit for making switch networks must have at least twice that many, and preferably four or eight times, so the importance of a narrow data path becomes obvious. Actually, the 16 data bits will be accompanied by a clock, a flag bit, and probably a parity bit, so the numbers are somewhat larger than stated above.

Modern ECL circuits appear to be able to handle point-to-point transfers at these data rates, but some care will be required

with layout and connectors.

We are addressing the logical problems in several ways, trying to keep the system efficient by appropriate choice of protocols and trying to prevent starvation, or deadlocks by providing forward-progress mechanisms.

The protocol efficiency can be affected by the format of the packets, which should be designed to provide the information in the best way for very fast processing in the interface; by the command set, which should not only match the needs of SCI but also provide the necessary mechanisms for communicating with other buses through interfaces from SCI; and by the choice of interprocessor communication primitives, the semaphor or lock mechanisms.

We are assuming 64-bit addressing, with the high 16 bits used for module selection (to be examined at very high speed).

SCI packets transfer a minimum of 16 bytes, but permit use of any contiguous subset. SCI also supports aligned block transfers of 32, 64, 128 and 256 bytes. The 16-byte packet provides for lock operations on 1, 2, 4 or 8-byte variables. The supported locks are *load and store*, which returns the original value and stores the new one; *load and add*, which returns the original value and adds the provided increment; and *test and store*, which returns the old value and if it matches a test value replaces it with a new one (useful for linked-list append).

Forward-progress mechanisms try to guarantee allocation of resources in such a way that large classes of trivial deadlocks cannot occur. For example, some sort of emission control is needed to prevent one user from hogging all of the data transmission capacity of a switch trunk or an insertion-ring "backplane." Some sort of selective acceptance of packets is necessary to prevent a saturated popular server from devoting all its resources to one user. And, some rejection mechanism may be needed in order to free space in filled queues for more important traffic. Separate queues are maintained for requests and responses, so that an overload of requests cannot block the responses which must be sent in order to free server resources.

We are developing a cache coherence mechanism which maintains a distributed directory of users of each data item, so that only those who care have to be notified when shared data is modified. By storing this directory as linked-list pointers in each participating cache, the storage required does not have to be preallocated and there is no intrinsic limit to growth.

The proposed mechanism seems simple enough that it should work, but it is not trivial. We must carefully check corner cases, such as what happens if one node decides to remove itself just as another is trying to add itself onto the list. Additional system traffic is required for maintaining coherence, but it is proportional to the information transfer traffic (about double for cached items). This seems a reasonable cost in exchange for the much larger factor of parallelism it makes possible, and for moving spin-wait traffic into caches.

Acknowledgements

Conclusion

The SCI project is moving rapidly, and has attracted participants from many of the high-performance computer companies. The proposed signalling mechanisms appear to be technically feasible (though not entirely trivial), and there appear to exist logical protocols which are compatible with our goals.

The next phase will be a more careful study of the effects of various compromises and optimizations that could be applied to our logical protocols, and the selection of suitable connectors and packaging mechanisms. There is a lot of work to be done, but the enthusiasm level is high and progress has been rapid, so we are optimistic that we can achieve a workable specification in record time.

If you would like to participate in this work, or if you would like more detailed information, please contact the author:

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Scalable I/O Architecture for Buses

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ABSTRACT

Current IEEE activities on the P1394 bus standard (1 Mbyte/sec) and the P1596 interconnect (1 Gbyte/sec) are in the process of defining standard control register locations, formats, and functions. This scalable definition, called an I/O Architecture, is being considered for use by other bus standards as well (P896.1 Futurebus and the P1014 VME bus standards).

The scalable I/O Architecture definition is bus-technology independent, and supports large multiple-bus configurations. Several of the scalable features of the I/O Architecture are described.

1 INTRODUCTION

1.1 SCALABLE BUS ARCHITECTURES

A scalable bus architecture can be applied to a wide range of bus technologies. One of the low cost buses under development is the P1394 Serial Bus standard. The serial bus is intended for use with existing backplane buses. It provides a redundant communication path, which can be used to diagnose errors when the primary parallel bus fails.

The serial bus is extendable to several backplanes, but transceivers are required to translate the backplane-specific signal levels to the standard external signal levels, as illustrated below:

Low-Cost Interconnect

Chassis A   Chassis B

P1394
(Serial Bus)
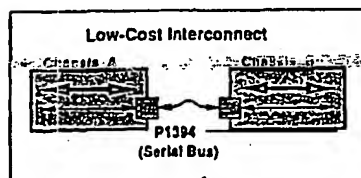
Another example is the P1596 Scalable Coherent Interface (SCI). This is one of the highest-performance bus standards under development. This 1 Gbyte point-to-point connection standard is intended for use in high-performance work-stations and supercomputers. A supercomputer could be built using boards designed originally for high-performance work-stations. To avoid the traditional shared-bus bandwidth limitation, an active switch is used to interconnect the SCI boards, as illustrated below:

High-Performance Interconnect

Active Switch

node[0]   PC-Boards
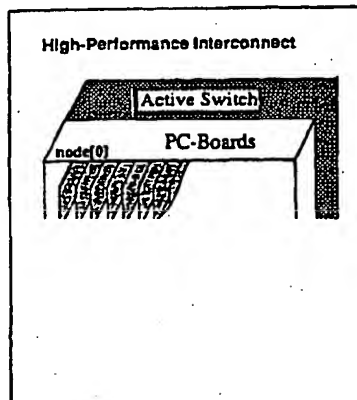
The proposed SCI standard defines the interface between each of the boards and the active switch.

These two interconnect standards share the same I/O Architecture. By applying the I/O Architecture across this wide performance range, the scalability of the I/O Architecture has been well tested.

1.2 SCALABLE COMPONENTS

The foundation of the I/O Architecture is the set of bus operations used to transfer data and control between nodes attached to the bus (or bus-like interconnect).

Some of the existing bus standards provide complex bus operations, such as doubly-linked-list-insert. These are hard to implement on higher-speed buses, or across large multiple bus system configurations.

Other buses lack the basic bus lock operations, such as the load_store operation, which is necessary to synchronize the operation of multiprocessor systems. As a basis for the

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following I/O Architecture, a scalable set of bus operations is presented.

Scalability is partially defined by the number of functions on a board, and the number of boards in the system. With the dropping costs of VLSI circuits, multi-function boards are now the norm, rather than the exception. At experimental research facilities, large systems have hundreds of data-collection boards. The proposed I/O Architecture can support either a large number of functions on a node, or a large number of nodes in the system.

Scalability is also defined by the efficiency of I/O transactions. A scalable I/O Architecture should reduce the number of processor interrupts per disk I/O, and reduce the dispatch time for each interrupt. The proposed DMA-chaining architecture has both of these properties.

2 BUS OPERATIONS

A scalable set of bus operations must support existing bus standards, current uniprocessor designs, and the future multiprocessor systems. All of these capabilities can be supported with a small set of bus operations.

Scalable bus operations have two phases. The request phase is used to transfer the address and command from the requester to the responder. The response phase is used to return the status from the responder to the requester. Depending on the bus operation, data may be transferred in the request phase, the response phase, or both, as illustrated below:

Bus Operations

	Request	Response
Block read:	head	head 32-256
Block write:	head 32-256	head
Selected read:	head	head 16
Selected write:	head 16	head
Selected lock:	head 16	head 16
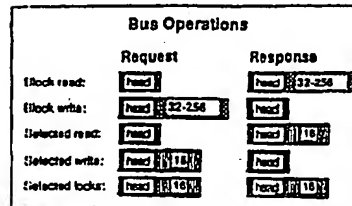
On slower buses, such as the P1394 serial bus, the request and response phases can be merged. On higher-performance interconnects, such as the P1596 SCI standard, this is not possible.

Block read and write operations are required to efficiently support cached based processor systems. The block transfer sizes are 32, 64, 128, or 256 bytes. The address of a block transfer is always aligned to the block size. Larger block sizes could have been implemented, but they would unnecessarily complicate the protocols for a minimal improvement in bus bandwidth.

Small byte, doublet, triplet, quadlet, and other contiguous-byte operations are needed by the bus adapters which connect to existing bus standards. These sub-block operations are implemented by sending 16 bytes of data, but selecting the contiguous range of affected bytes. This byte selection capability is illustrated below:

Selected-Byte Operations
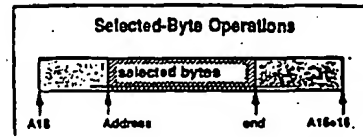
Within the 16-byte block, any contiguous range of bytes may be affected.

On many of the existing bus standards, lock operations are implemented as an indivisible sequence of bus operations: bus ownership is maintained while the operation sequence is being performed. This is cost-effective for a single-bus system, but impractical for large multiple-bus system configurations.

A preferred technique is to implement the indivisible updates at the data location. The operation command specifies the actions to be performed. The following three lock operations are defined:

Lock Operations

OP	Action
load_store	new= set
load_add	new= old+set
test_store	if (test==old) new= set
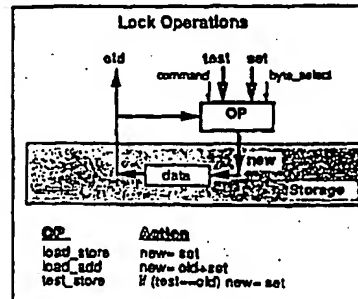
The load_store lock is necessary for compatibility with existing buses. By sending ones or zeros to the responder, either of the popular test&set or load&clear bus operations can be emulated.

The load_add lock is very useful for allocating shared resources. With the proper active switch design, load_add can also eliminate hot-spots in the switch interconnect.

The test_store lock operation is used to perform indivisible linked-list inserts. This simplifies multiprocessor software, and is necessary to implement the scalable DMA architecture.

3 NODE ADDRESSING

3.1 ADDRESS-SPACE PARTITIONING

A scalable I/O Architecture should be auto-configurable and support configurations with large numbers of bus nodes.

For the 64-bit address space of the proposed P1596 SCI standard, the total address space is large enough to be equally partitioned for the maximum number of nodes in the system, as illustrated below:

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64-bit Node Addressing
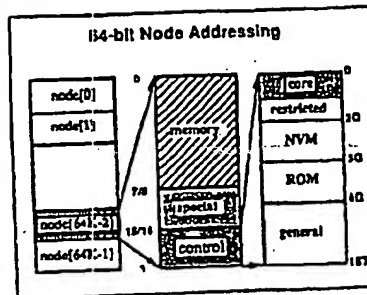
The upper two bytes of the 64-bit physical address space select one of 64K nodes. Each node allocates a small portion of its address-space for standardized control registers.

The standard control registers are used to identify, initialize, and control the node hardware. The control register address space is sufficiently large to directly map any reasonable size of identification ROM (which identifies the node and specifies its capabilities) or non-volatile memory (which saves configuration parameters for the next system boot-up).

The 32-bit physical address spaces of the P1394 serial bus cannot be equivalently partitioned. If equally allocated, the maximum size of the node address space (64Kbytes) is insufficient to directly map the address space of memory controller RAM.

To efficiently utilize this 32-bit physical address space, only a small portion (1/16) of the address space is allocated for the node's initial physical address space, as illustrated below:

32-bit Node Addressing
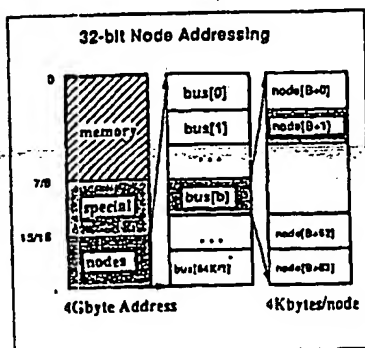
Since the node's initial address space is small (4Kbytes in size), extended address-space modes are provided. The lower ROM address can be mapped directly into a portion of the node's initial address space. Other ROM addresses are accessed indirectly, through a ROM address-window.

Extended addresses are used to direct map memory-controller RAM. This address-space is dynamically assigned, by writing to an extended address register in the node's initial address space.

3.2 BOARD ARCHITECTURES

A node is the architectural entity, which can be identified, reset, and tested independently. A board, which is purchased and replaced as a unit, may consist of one or more nodes. This is illustrated below:
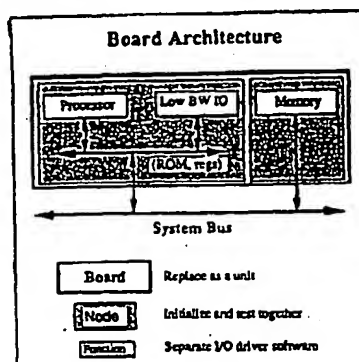
The number of node addresses on a board is bus-standard dependent. Typical values on existing or evolving backplane bus standards are 2, 4, or 8 nodes per board.

The core of the node address space provides generic facilities for identification, reset, and test. In addition, the node address space is also partitioned into one or more application-specific functions.

A function contains the registers accessed by specific I/O driver software. Examples of functions include multiprocessors, memory, and RS-232 MUX adapters.

3.3 SUB-FUNCTION PARTITIONING

Except for specialized boot device architectures, the detailed definition of I/O functions is beyond the scope of the I/O Architecture. However, the expected implementation model has influenced the I/O Architecture design.

A multiplexed function (such as a multiprocessor, terminal multiplexer, or disk controller) would be mapped to multiple register-sets. One shared register set controls the shared facilities.

Separate register sets are used to control each of the attached devices. A SCSI disk adapter function, for example, would allocate one register set for each disk. This disk controller register set partitioning is illustrated below:

Independent Device Register-Sets

Register Sets

disk[7]
disk[5]
...
disk[2]
disk[1]
control

▨ Device Register Sets
▥ Central Control
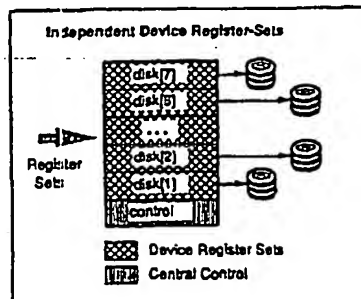
On full-duplex devices, such as an RS-232 terminal, a separate register set is assigned for the input and output channel of each duplex connection.

4 DMA AND INTERRUPTS

4.1 PROCESSOR INTERRUPTS

On many of the existing bus standards, specialized hardware sends interrupts to the processor from an I/O adapter. Other bus standards have memory-mapped interrupts; the interrupt is directly mapped to a write operation on the bus, as illustrated below:

Simple Uniprocessor Interrupts

Processor — Interrupt reg — write (busy) — I/O Adapter
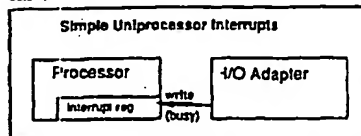
On a processor with vectored external interrupts, the interrupt data specifies the interrupt priority and the vector dispatch address.

Most vectored interrupt schemes scale poorly. When multiple interrupts are sent, the acceptance of lower-priority interrupts is delayed while the higher-priority interrupt is processed. For memory-mapped interrupts, the delay is generally implemented by terminating the write with a "busy" status. The busy write operation is retried until accepted.

The delayed acceptance of interrupts could deadlock multiprocessor systems. For example, an interrupt service routine sends a lower-priority interrupt to another processor. When two processors execute this routine simultaneously, the system deadlocks, as illustrated below:

Deadlocking Multiprocessor Interrupts

Processor — Interrupt reg — writes (busy) — Processor — Interrupt reg
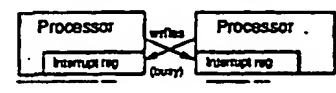
To avoid deadlocks, interrupt parameters are always queued, but the interrupt processing may be delayed.

To implement generalized vectored interrupts, the size an interrupt parameter queue would be excessive. For this reason, the queue only holds the interrupt priority level. The interrupt dispatch address is specified by shared data structures in memory.

4.2 DMA CAPABILITIES

4.2.1 Historical Perspective

DMA (Direct Memory Access) is simply the transfer of data in or out of system memory under control of the I/O Adapter without the involvement of a processor. In the simplest form, a data address and transfer length register are used to specify the location and length of a contiguous data transfer.

On a virtually addressed system, contiguous DMA transfers are inefficient. Most transfers involve a large contiguous virtual address space, which must be split into many smaller transfers to contiguous physical addresses. The processor is interrupted between each of the small data transfers.

To eliminate these unnecessary interrupts, additional DMA hardware capabilities, called address chaining, are often provided. This DMA hardware includes the capability of fetching data transfer commands from memory, based on a command-list pointer initialized by the processor. The use of this capability is illustrated below:

DMA Data-Chaining

I/O Adapter — dma_start — (2) — Processor

(3)

add0 add1 addN

page0 page1 pageN

Memory

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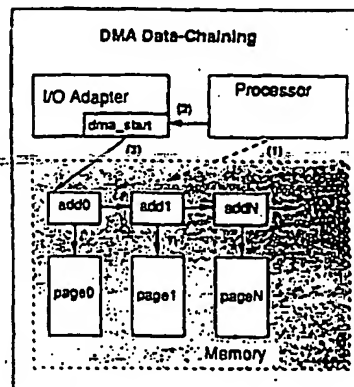
The DMA operation is initiated as follows:

1. **Memory setup.** A linked-list of data transfer commands is written to memory.

2. **DMA_start.** The processing of the linked-list is initiated by a write to the I/O adapter's dma_start register.

3. **DMA processing.** The I/O adapter fetches its data-transfer commands from memory. It then transfers data to (or from) the specified address ranges.

The address-chaining capability improves the performance of DMA operations, but still limits DMA processing to a single DMA request. This is a significant performance limitation for many high-performance devices, and overly complicates the design of real-time data acquisition systems.

4.2.2 Proposed DMA Architecture

To process multiple DMA requests, the DMA adapter must be able to fetch its commands from memory, without processor intervention. Also, the completion status from one request must be saved before the command entries from the next DMA request are processed. This is accomplished by enhancing the format of the DMA chaining structure in memory, to include the command and status entries. The enhanced command-list structure is illustrated below:

DMA Request Structure

DMA Requests

| Request_1 | Request_2 | Request_3 | ... | Request_N |

| pointer | cmd | pointer | cmd | ... | pointer | cmd |

| arg_1 |
| arg_2 |
| arg_3 |

Initialize   Data Transfer   Status
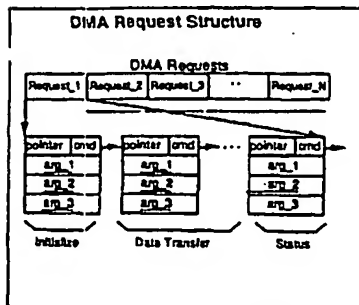
Within one priority level, the processing of DMA commands is now based on two lists. The command list is constructed by processor software and contains the DMA commands to be executed. The status list is constructed by DMA hardware, and contains the status of the completed DMA operations.

The same steps are used to initiate the DMA activity, as illustrated below:

DMA Request Chaining

I/O Adapter   Processor

dma_start

cmd   add0   list

command list

page0

HW status
SW status

head   statB   statC

status list

Memory
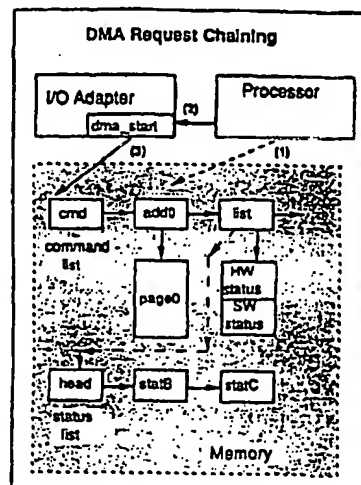
In this example, the status list is shared by other DMA command lists, which have previously inserted statB and statC entries into the status list.

After a request has been processed, the previously assigned status entry is updated and inserted at the head of a memory-resident status list, as illustrated below:

DMA Request Chaining

I/O Adapter — dma_start — Processor

interrupt (4)

(5) (continue...)

cmd   add0   list

command list

page0

head   HW status   stat9

SW status
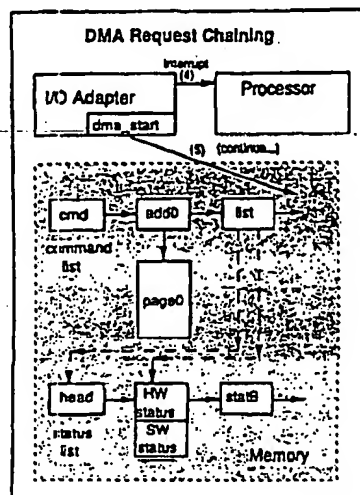
status list

Memory

Since the hardware status has been copied to memory, processing of additional DMA commands can safely continue.

The new status entry is inserted into the status list using the test store lock operation. The status list is maintained in a LIFO (last in, first out) order. Although software would prefer a FIFO (first in, first out) ordering, this is harder to implement.

By software convention, the status list may also contain data provided by the I/O driver software. This information generally includes the interrupt-dispatch address and parameters. Using this information, interrupts can be efficiently dispatched.

In large system configurations, the status-list dispatch is much more efficient than polling the I/O cards to determine the interrupt cause.

5 OTHER SCALABLE FEATURES

The most important features of the scalable I/O Architecture have been discussed. There are other features which improve scalability of an I/O Architecture as well; these will be described briefly.

All of the standard control registers are defined to be 4 bytes in size, and are 4-byte aligned. These registers can be manipulated by 32-bit RISC processors, which only support word load and store instructions. The 4-byte access mode also minimizes the incompatibilities when a little-endian processor is attached to the big-endian I/O Architecture.

All nodes on the bus have an identification ROM, which identifies the node and describes its capabilities. By properly encoding the first word in ROM, the architecture allows an implementation to map 1, 2, or 4 bytes of ROM into each of the 4-byte control registers. A byte-wide ROM can attach to the most cost-effective byte location.

Boot devices (operational capabilities, commands, and status) are fully defined device architectures, which use the standardized DMA facilities. Alternative architectures, which locate the boot-device code on the processor or I/O board, are highly processor instruction-set dependent.

The time required to complete a self-test command may range from a few seconds to several minutes. For self-tests which exceed a few seconds, a forward-progress register is updated periodically. By reading this register, a failure in a long self-test sequence can be detected as quickly as a failure in a short self-test sequence.

6 CONCLUSION

It is often tempting to specialize the definition of bus operations and I/O Architectures to specific hardware implementations. This reduces the localized design effort, because implementation-specific solutions are usually the easiest to discover. However, major software rewrites are required to migrate between system bus standards.

A preferred solution is to invest the time initially, by developing a scalable bus-technology independent I/O Architecture. For the proposed IEEE P1394 and P1596 standards, this design approach has been effective. Participants in several other standards have also expressed interest in this design approach.

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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	2 May 2000	Nguyen Xuan Hiep, C

863 FH PG 0540

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The members are as contained in the European Patent Office EDP file on
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02-05-2000

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G 06 F 13/42
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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	12-02-1990	NGUYEN XUAN HIEP C.

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Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.4)
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Place of search	Date of completion of the search	Examiner
THE HAGUE	25-04-1990	DE LA FUENTE DEL AGUA Y.

EPO FORM 1503 03.82 (P0401)

BNSDOCID: <EP___0246767A3_I_>

New System Architectures for DRAM Control and Error Correction

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INTRODUCTION

Dynamic Random Access Memories (DRAM) have evolved from moderate-performance, low-cost storage media into versatile solutions for a wide range of applications. The better AC performance, the greater density, and the variety of architectures and access modes are drawing more system designers to replace alternative storage media with DRAM arrays.

Wider data paths in microcomputer systems and new DRAM densities exhaust the capabilities of the first-generation DRAM controllers, thereby giving rise to the need for cost-effective, high-performance new solutions for DRAM control.

The physical dimensions, the signal levels, and the charge stored in the dynamic memory cells are greatly reduced to allow denser and faster DRAMs. With the shrinking dimensions, and the growing memory sizes, the memory systems are now more susceptible to soft errors; thus, more and more system designers resolve to include Error Detection and Correction (EDAC) circuitry in their systems.

This paper presents a new family of dynamic RAM controllers that provides economical solutions for DRAM systems. Also, a new family of Error Detection and Correction devices featuring the Flow-Through architecture is described and compared against the more common Bus-Watch architecture.

A DYNAMIC RAM SYSTEM

In a dynamic RAM system (see figure 1), special circuitry is needed in the address/control path to control the dynamic RAMs and interface to the CPU. This circuitry generates refresh address; it multiplexes row, column, and refresh addresses; and it drives the control signals to the dynamic RAMs. In addition, it initiates refresh cycles at the rate that is
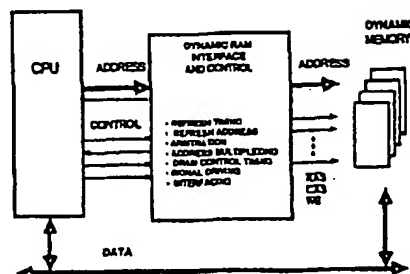

Figure 1. A Typical DRAM System

Most available LSI dynamic RAM controllers make an attempt to provide a complete "single-chip" solution for dynamic RAM control incorporating some interface and access/refresh arbitration circuitry in the controller itself. Unfortunately, the required timing and protocol for system memory access vary significantly from one CPU or system to another. The result is that in the effort to accommodate many different systems, performance is sacrificed. The "flexibility" of such controllers is actually the cause of their being complex, multi-mode, power-hungry devices. Furthermore, significant "glue" logic is still needed for the interface, as is evident from the elaborate application notes published with each and every controller. The complexity of the controllers, together with their slow speeds, has pushed many system designers to make their own controllers using "discrete" SSI/MSI devices.

* PAL (R) is a registered trade mark of Monolithic Memories.

THE 673104 FAMILY OF DRAM CONTROLLERS

Determining the optimal level of integration was a crucial task in the development of the new family of controllers from Monolithic Memories. The 67310X dynamic RAM Controller/Driver (Figure 2) provides all the dynamic RAM control functions that do not change from system to system. These functions are

- Refresh address generation
- Row, column, and refresh address multiplexing
- RAS, CAS, and WE control signals generation
- Memory array driving.

The control signal timing may be derived from external signals (Externally Controlled Access mode); or, for accessing 150ns and faster dynamic RAMs, it may be automatically generated by the controller itself (Automatic Access mode). To allow the system designer greater flexibility, no attempt was made to handle system-dependent handshake and arbitration functions.

The 67310X operates in three modes: Externally Controlled Access, Automatic Access, and Refresh. The Externally Controlled Access mode gives the system direct and flexible control over the RAS, CAS, and address outputs. In this mode the 67310X serves as a straight-forward multiplexer and driver for the address and control signals to the dynamic RAMs. The propagation delays and skews in this mode are specified to enable the system designer to arrive at any control timing sequence with great resolution. The Externally Controlled Access mode supports Page, Static Column, and Nibble mode accesses.

The timing parameters for each of the three controllers are specified for a load corresponding to 88 dynamic RAMs as well as for higher loads. The 673104 can drive and address 16Mbytes of dynamic memory organized in four banks of four bytes. The 673103 can address 8 Mbytes organized in four banks of two bytes; while the 673102, with 9 address outputs, can address 2 Mbytes. Table 1 exhibits the different controllers of the family.

Figure 2. 67310X Functional Block Diagram

	673102	673103	673104
SIZE OF DRAMS CONTROLLED	256K	1M	1M
NUMBER OF BANKS	4	4	4
NUMBER OF BYTES (PER WORD)	1	2	4
ADDRESS SPACE	256byte or 2M 16-BIT WORDS	8Mbyte or 8M 16-BIT WORDS	16Mbyte
PACKAGES	44-PIN DIP 44-PIN PLCC 44-PIN PPGA	52-PIN DIP 68-PIN PLCC 68-PIN PPGA	84-PIN DIP 68-PIN PLCC 68-PIN PPGA

THE PINOUTS FOR THE 44-PIN PACKAGES ARE UPWARD-COMPATIBLE ALLOWING A SYSTEM TO BE UPGRADED WITH MINIMAL WIRING CHANGES
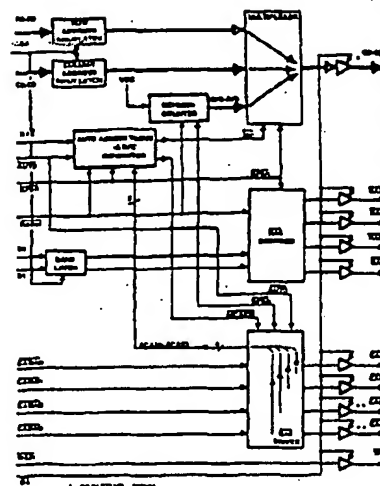
673102/3/4 FAMILY OF CONTROLLERS

MULTIPLE CASIN-CAS CANNELS SIMPLIFY LOGIC AND CUT PROPAGATION DELAYS

In any system with word-wide data (16-bit or 32-bit), either byte may be accessed, or several bytes may be accessed simultaneously. All currently available controllers have only one CAS output. When a single-CAS dynamic RAM controller is used to access word-wide memory, external logic is needed to split the CAS output coming out of the controller and create separate CAS signals for the separate bytes of the data word. Also, external drivers are needed to drive the CAS lines. The external logic adds to the system's chip count and lengthens the propagation delay of the CAS signals (see Figure 3). For example, in designs using a single-CAS controller, the added CAS delay is 40ns, which dramatically increases RASIN to CAS delay (t_{RICL}) and degrades system performance. The multiple CASIN-CAS input-output channels of the 67310X allow it to directly access individual bytes, or any combination of bytes, with no
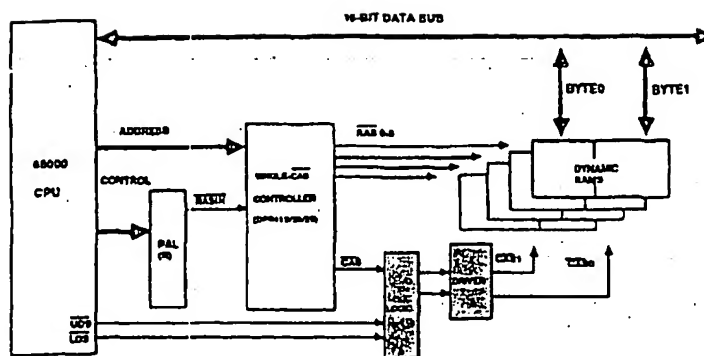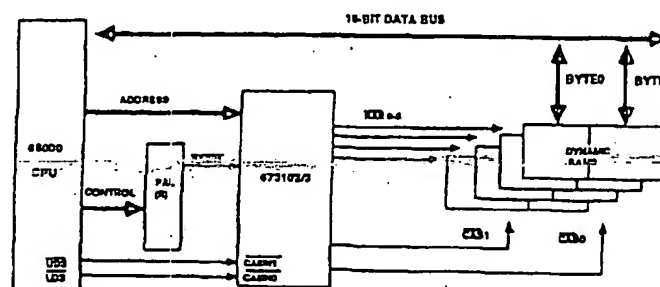
FIGURE 3. THE MULTIPLE CAS OUTPUTS OF THE 673102/3/4 USED FOR INDIVIDUAL BYTE
ACCESS SIMPLIFY THE LOGIC AND REDUCE PROPAGATION DELAY.

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4/3